IDEC Chip Design Contest

Characterization of 65-nm MOSFET and Wire Devices for Cryogenic Computing

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I. Introduction

Cryogenic computing, which runs computers at extremely low temperatures (e.g., 77K) has been emerged as a highly promising solution for the next-generation computing. To build the best cryogenic-computer systems, architects should utilize the accurate performance model based on the cryogenic MOSFET and wire properties.

In this project, we fabricate MOSFET and wire samples with Samsung's 65nm technology and measure their 77K properties to improve model's accuracy. Next, we measure our samples' I_{on} and and wire resistance with the semiconductor analyze. We also compare our 65nm results with our previous 28nm measurements. Our analysis will greatly contribute to developing more accurate models for cryogenic computing.

II. Design and Implementation

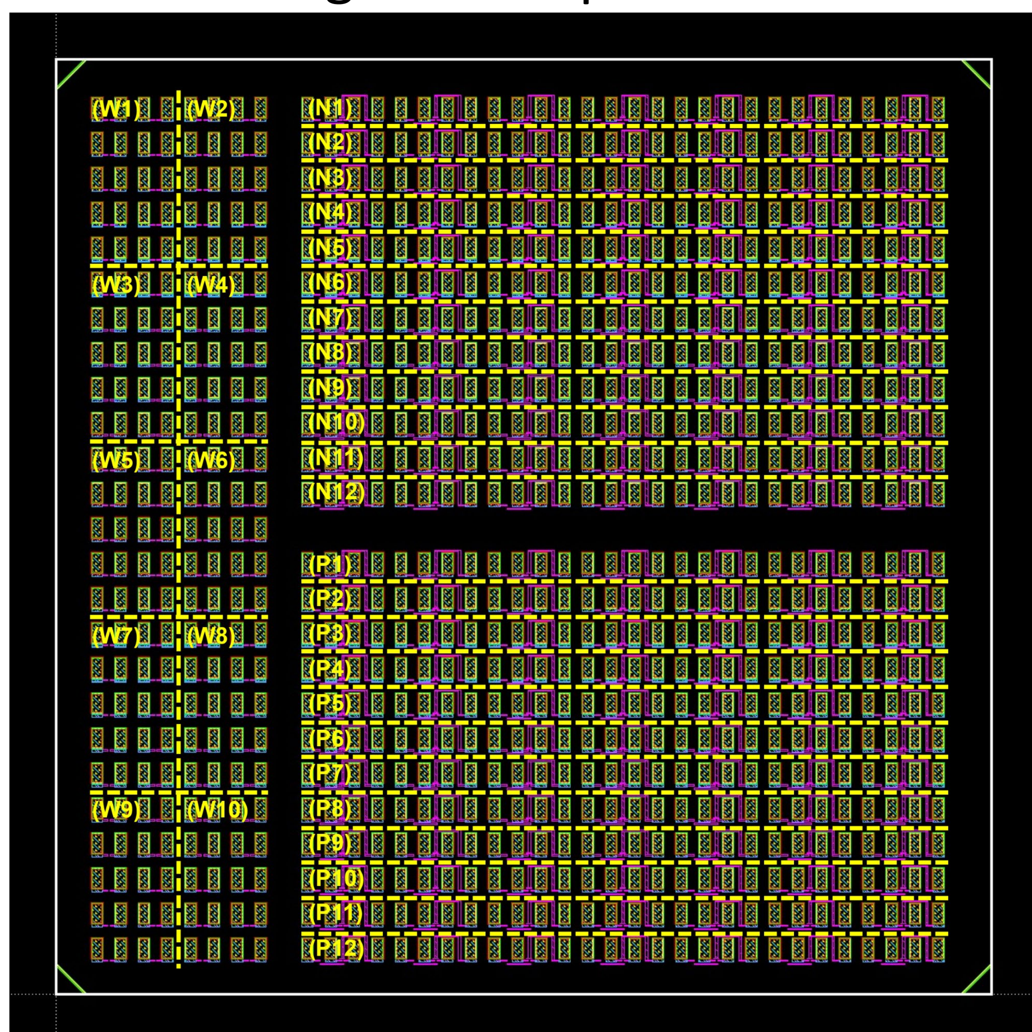


Figure 1. Layout of designed 65nm MOSFET and wire samples

Fig.1 shows the layout of the fabricated MOSFET and wire samples, which include 100 wire and 168 MOSFET samples with various wire length and gate width, respectively. For the wires, we fabricate ten types of wires whose wire lengths range from 90nm to 900nm, with the 90nm interval (W1 to W10). For the MOSFETs, we fabricate 12 types of samples whose gate widths range from 210nm to 2520nm with the 210nm interval (N1/P1 to N12/P12).

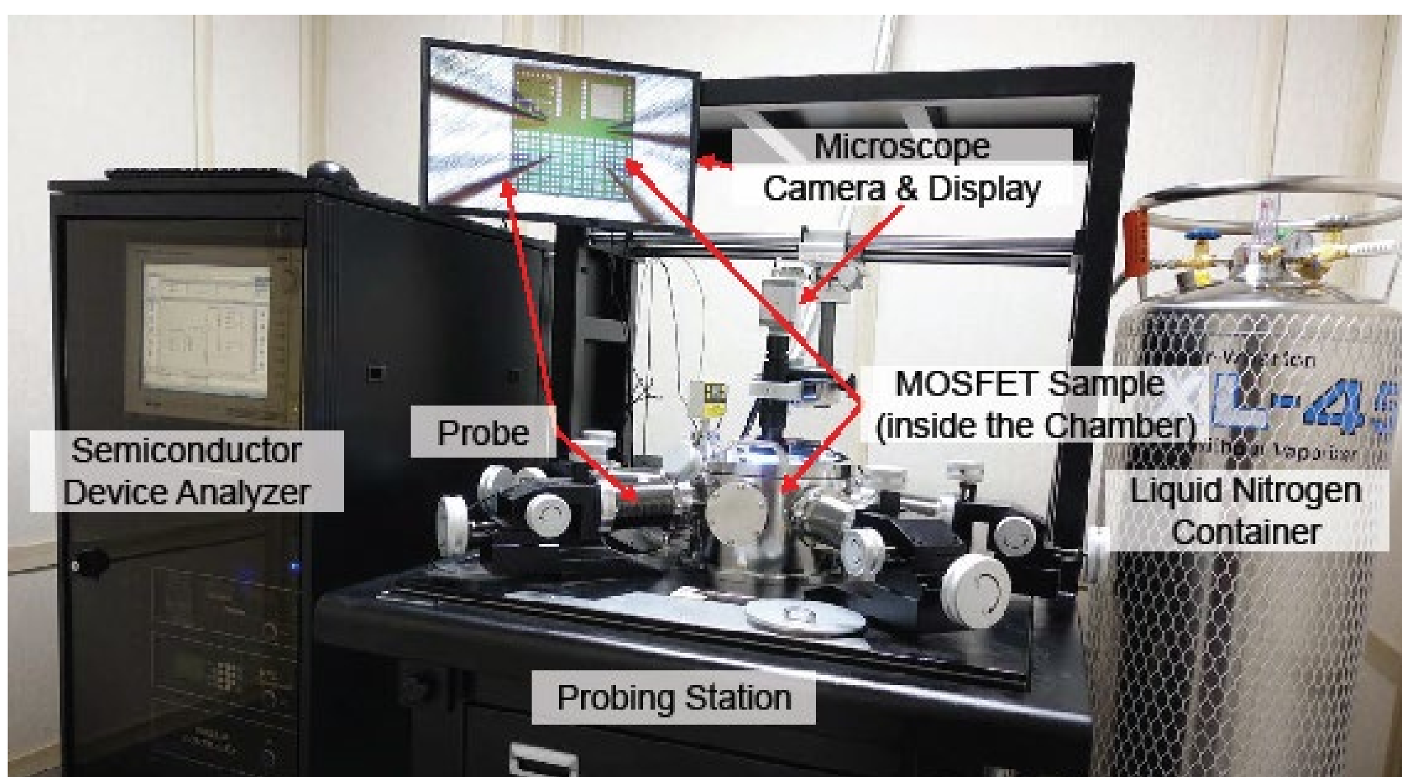
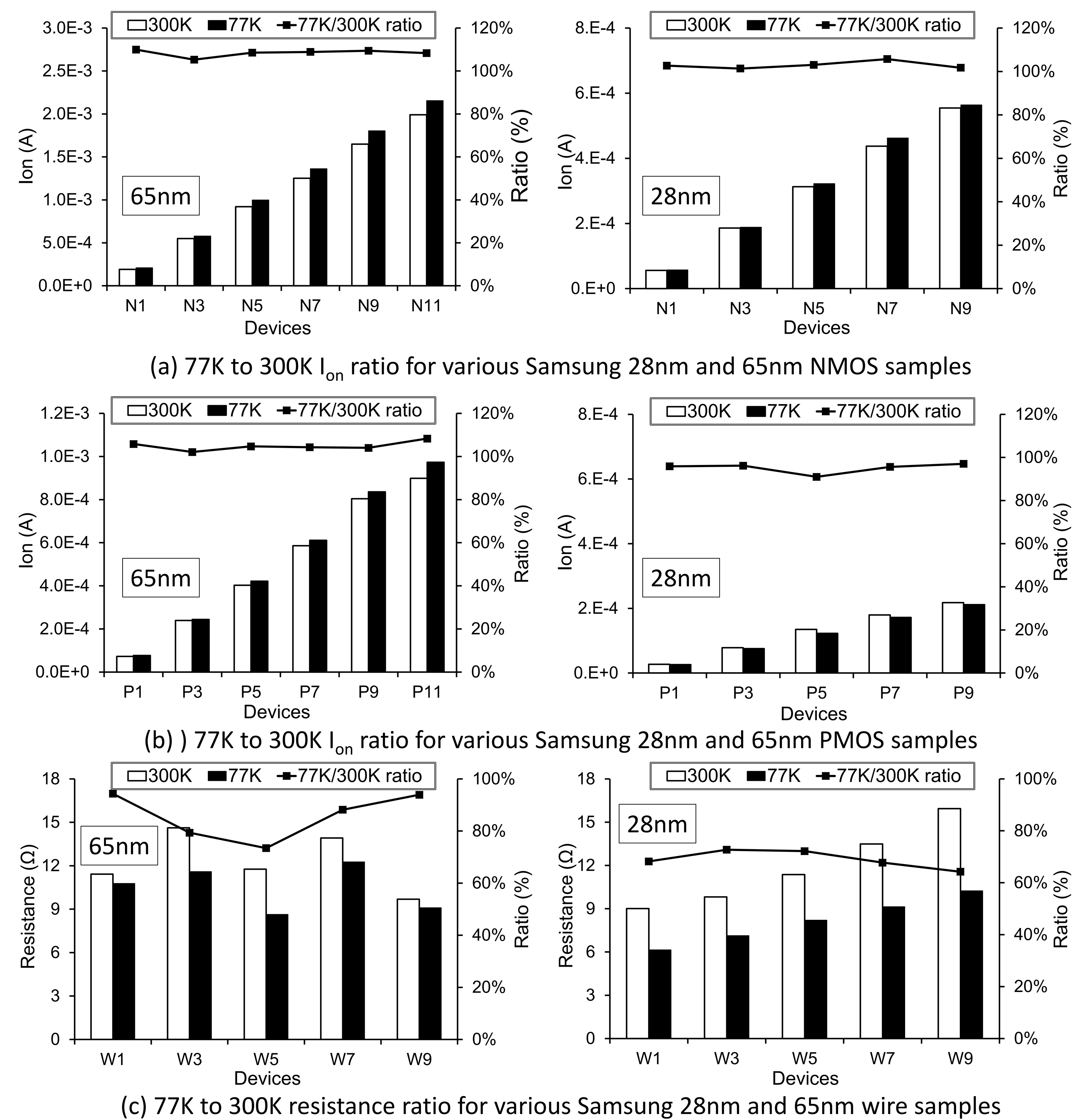


Figure 2. Experimental setup to measure MOSFET and wire samples at 77K

Fig.2 shows our measurement setup to measure the MOSFET and wire characteristics at 300K and 77K. We utilize a custom-built MOSFET probing station, which consists of a Keysight B1500A semiconductor device analyzer and a liquid nitrogen (LN)-based cryogenic cooling unit.

III. Measurement result



(a) 77K to 300K I_{on} ratio for various Samsung 28nm and 65nm NMOS samples

(b)) 77K to 300K I_{on} ratio for various Samsung 28nm and 65nm PMOS samples

(c) 77K to 300K resistance ratio for various Samsung 28nm and 65nm wire samples

Figure 3. measured 77K to 300K ratio for (a) NMOS, (b) PMOS and (c) wire samples

Fig.3 shows the measured 77K to 300K ratio for (a) NMOS, (b) PMOS, and (c) wire samples of Samsung 65nm and 28nm technology, respectively. We summarize our key observations as follows.

1. **NMOS/PMOS at 77K.** As shown in Fig.3(a) and Fig.3(b), we observed that the on-channel current (i.e., I_{on}) slightly increases with the temperature reduction. For 65nm technology, Ion of NMOS and PMOS increases at 77K by 8.4% and 4.8% on average compared to the 300K value. On the other hand, in our previous measurement for 28nm technology, the I_{on} improvement is lower than that of 65nm technology (2.9% and -4.9% for NMOS and PMOS). In addition, we observe that gate width does not meaningfully affect the temperature dependency of I_{on}, with 4.4% and 6.6% of maximum difference on 77K-to-300K ratio for 65nm technology.
2. **Wire at 77K.** As shown in Fig.3(c), we observe that the wire resistance is greatly reduced at 77K, but the resistance reduction is much lower than that of the bulk copper. The average wire resistance reduction is 20% in 65nm technology, while the reduction in bulk copper is 85%. For 28nm technology, the wire resistance reduction is also lower than that of the bulk copper, but its trend is quite different compared to the 65nm results. Therefore, we plan to conduct the further measurements for more wire samples as our next projects.

IV. Conclusion

In this project, we measured and analyzed 65nm technology node's MOSFET and wire characteristics at 77K, to build more accurate cryogenic MOSFET and wire models. We observe the slightly higher I_{on} for both NMOS and PMOS, and significantly reduced wire resistance at 77K.

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