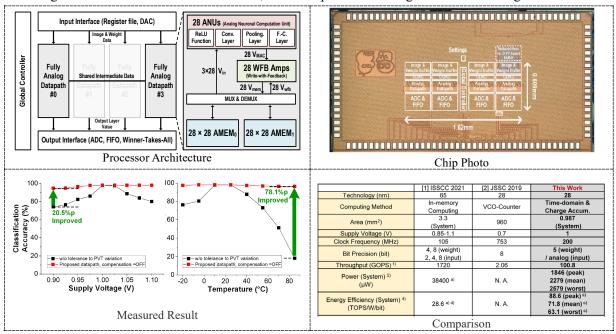
Energy-Efficient Neural Network Processor Using All-Analog Computation

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The increased complexity of machine learning algorithms and the development of powerful hardware accelerators that support them have greatly improved the performance of multimedia recognition. However, as the demand for low complexity in low-power sensor nodes and mobile devices has recently increased, edge computing, which means machine learning operations in edge devices, is drawing attention. The basic operator of machine learning is MAC (Multiply-and-Accumulate), and the multiplication operation is among the most complex digital arithmetic operations. Accordingly, recent studies have shown that analog-based operation circuits rather than existing digital-based operation circuits are more advantageous for low-power operations required by edge computing. In this work, we propose an energy-efficient CNN processor based on an analog internal circuit that takes analog raw data without ADC from the image sensor device as input. The proposed processor is designed based on IDEC MPW SS28-2101. It uses 1.0V as the supply voltage, the standard voltage of the 28nm LPP process, and operates at a frequency of up to 100MHz. In the case of the MAC circuit, it is based on analog, but from the point of view of the entire circuit, it is planned to be mixed with digital circuits for I/O and control units, so the chip has been designed with mixed-signal circuits.



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References [1] Chen, ISSCC 2021 [2] Toyama, JSSC 2019