IDEC Chip Design Contest

IDEC S28-2202 CDC

Triple-stacked Wideband Power Amplifiers Using CMOS 28 nm Process

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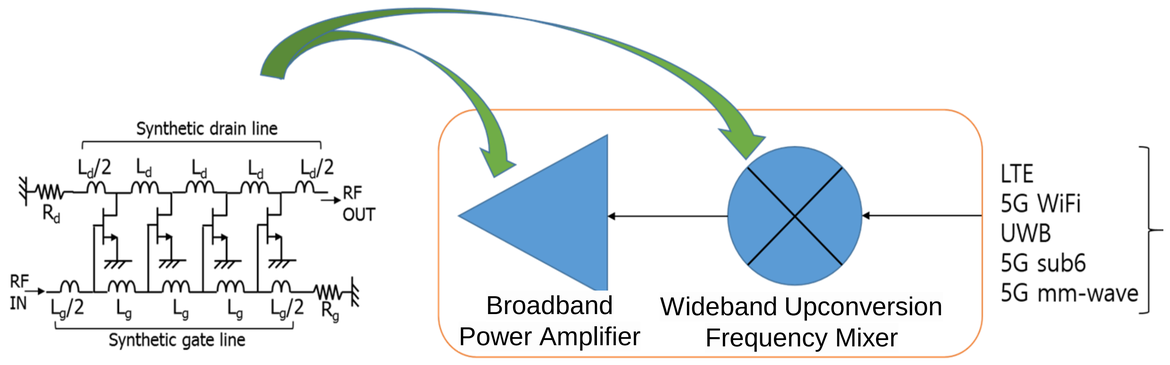
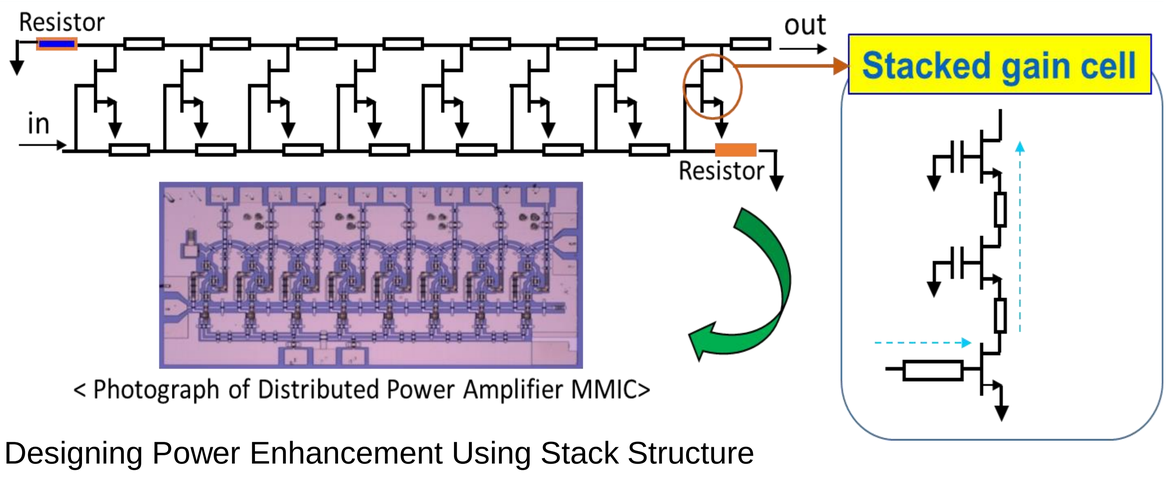
Introduction



- Design a wideband transmitter circuit using a distributed amplification method
- LTE, WiFi, UWB, 5G communication bands used →v Aim to obtain available output power via broadband power amplifiers of 1 to 40 GHz

Design



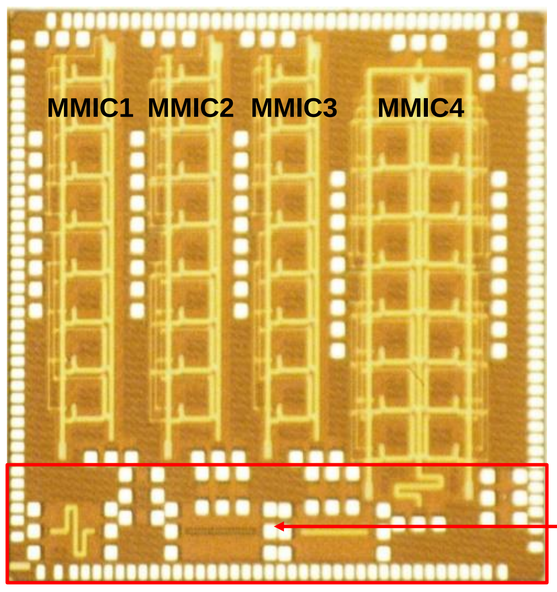
< Photograph of Distributed Power Amplifier MMIC>

Designing Power Enhancement Using Stack Structure

Low breakdown voltage of CMOS results in low voltage swing, limiting output power

-> Stacked FET structure improves voltage swing

- The number of stacks is determined by the cutoff frequency and maximum oscillation frequency of the cmos process
- In this design, 3 lvt_nfet_rf elements are stuck in consideration of 1 to 40 GHz operating frequency



- MMIC1: Use symmetry type lvt_nfet_rf
  Both gate bias and drain bias use a bias tee
- MMIC2: Use symmetry type lvt_nfet_rf
  Drain bias use a bias tee
- MMIC3: Use ring type lvt_nfet_rf
  Both gate bias and drain bias use a bias tee
- Passive element: CPW transmission line
  - ❖ MMIC: Monolithic Microwave Integrated Circuit
  - ❖ CPW: Co-planar Waveguide

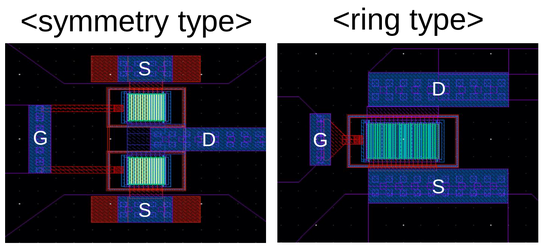
- S28-2202 MPW DB Design Manufacturing Circuit Description
- MMIC1: Use symmetry type lvt_nfet_rf
  Both gate bias and drain bias are designed to use external vias
- MMIC2: Use symmetry type lvt_nfet_rf. Drain bias use external bias tee
- MMIC3: Use ring type lvt_nfet_rf
  Both gate bias and drain bias are designed for external vias
- MMIC4: Structures of power combining of single power amplifier MMIC
- MMIC: Active and passive devices are circuit forms implemented on a single semiconductor substrate
- At the bottom of the Chip Floor Plan, passive element test pattern is implemented through Co-Planar Waveguide to check the performance and accuracy of the passive element of the semiconductor chip
- Passive element designs CPW transmission lines
- CPW: A transmission line with a certain distance of GND on the side parallel to the transmission line

Results

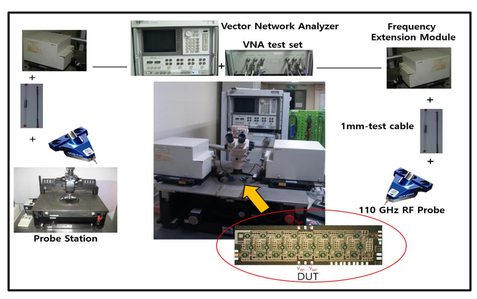
MMIC1 Layout

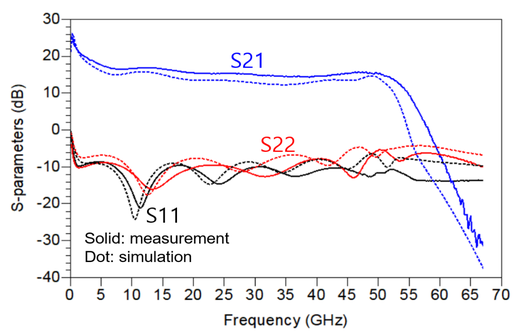
- FET: lvt_nfet_rf 2 × 32μm (total width 64μm)
- Size: 3000μm × 750μm
- 8 stage design with 3 stacked gain cells

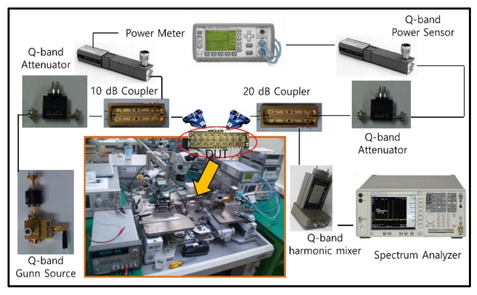
<symmetry type> <ring type>

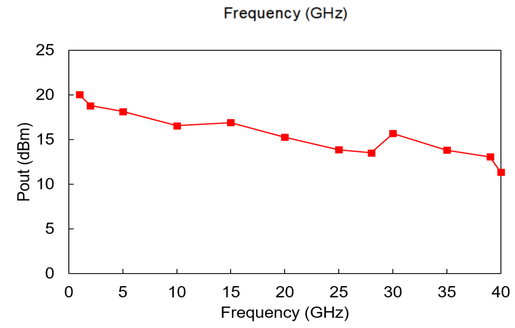


Measurement Result (S-parameter)









Measurements were made by setting VDD 4.0V, VGG 3.0V, VGG 2.6V, and VGG1 to 0.7V

- Small Signal: S21 of 10dB or more is maintained from 0 to 56GHz, and the maximum value is 16dB at 50GHz
- Large Signal: Output power of 14 dBm or more from 0 to 30GHz, 1GHz – 20dBm, and 30GHz - 15.7dBm

Ref	Technology	BW(GHz)	Gain(dB)	P_{sat}(dBm)	DE(or CE) (%)	Chip area (mm^2)
[1]	130nm SiGe	14 – 105	6 – 12	4 – 17	2 – 15.1 (15.1@50 GHz)	1.51
[2]	22nm FD SOI CMOS	0.4 – 31.6	11.6	14.5 – 16.4	11 – 17.2 (17.2^2@15 GHz)	1.50
[3]	45nm SOI PMOS	DC – 120	16	17 – 23	6 – 24 (18@50 GHz)	1.32
[4]	130nm SiGe	DC – 110	10	12.5 – 17.5	5 – 16 (16@60 GHz)	2.18
[5]	65nm CMOS	0.5 – 38	11 – 15.7	12.8 – 21.8	3.3 – 35.3 (17.9@10 GHz)	3.30
This work	28nm CMOS	0.1 - 56	10 – 16	11.3 – 20	3.7 – 19	2.25

Conclusions

In this study, the characteristics of the broadband distributed power amplifier were verified by measuring the S-parameter and output power for MMIC1, which was manufactured with the symmetric type NFET and the ring type NFET.

The fabricated distributed power amplifier maintained an S21 of 10dB or more from 0 to 56 GHz as a result of small signal measurements and achieved a maximum value of 16dB at 50 GHz. From the large signal measurements, the output power was over 14dBm up to 30 GHz, with 20dBm at 1 GHz and 15.7dBm at 30 GHz.

Based on this design and measurement results, improvement work will be undertaken to further increase the broadband output power in the next MPW.

References

Jihoon Kim, "A Wideband Triple-Stacked CMOS Distributed Power Amplifier Using Double Inductive Peaking," *IEEE MWCL* (2019)