IDEC Chip Design Contest

D-band CMOS Vector Modulator-Based Phase Shifter for Millimeter-Wave Imaging System

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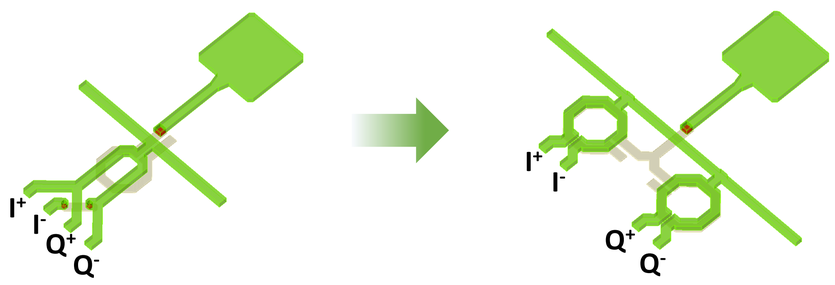
Motivate

● Millimeter-wave Imaging Systems using Polarization

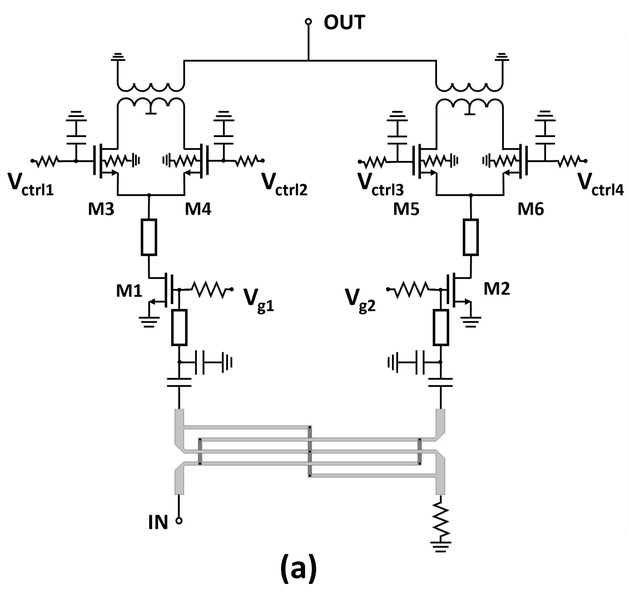
- By controlling polarization of transmitted signal, the detection of internal material properties at specific frequencies improves image quality.
- Due to the high attenuation of millimeter-waves in the air and high-transmission power is advantages in imaging systems, implementing a high-power transmitter is required.
- A high-power phase shifter capable of controlling transmission signal polarization is proposed for imaging systems.

Methods

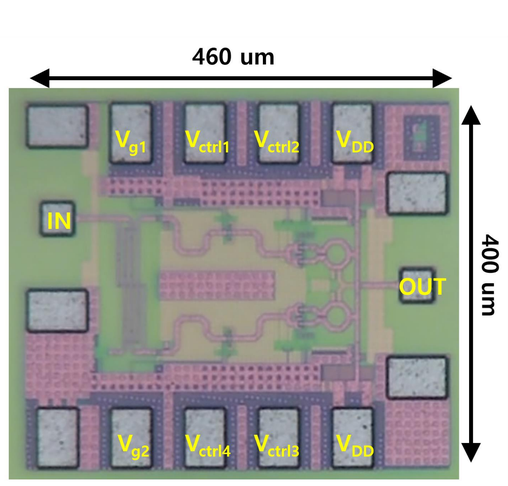
● Design of Vector Modulated type Phase Shifter



- By using Lange coupler, the low amplitude and phase imbalance I/Q signal is implemented with small sizes (60㎛x140㎛).
- The single Gilbert-cell configuration VMPS being simpler than the double configuration leads to low parasitic and improves gain.
- Placing a transmission line between transconductance and switching-cells enhances VGA gain and linearity by using resonance with parasitic capacitance [2].
- By modifying current direction, minimizing impedance variations caused by voltage control, and optimizing output impedance matching.



(a)

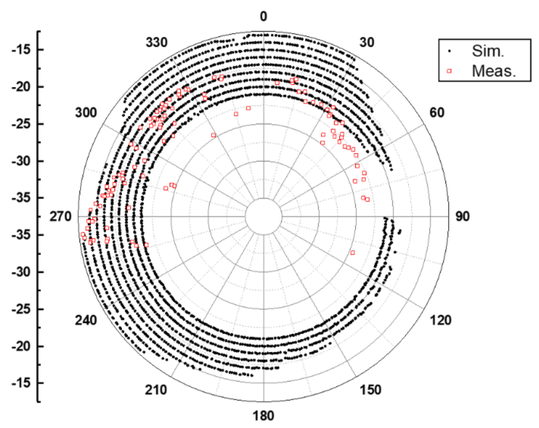


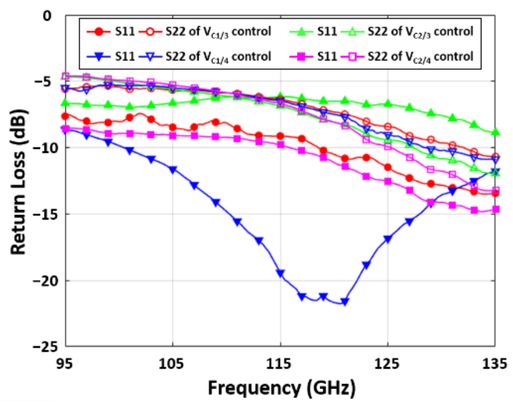
(b)

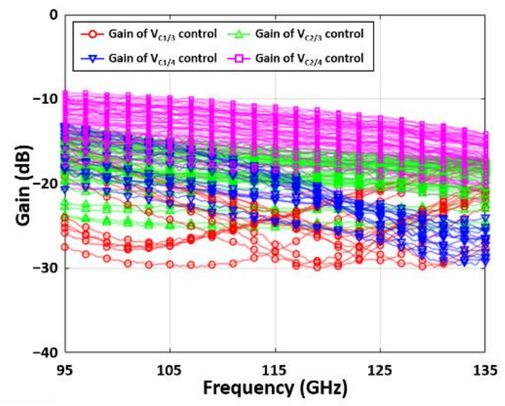
< (a) Schematic (b) Chip photograph of the proposed phase shifter >

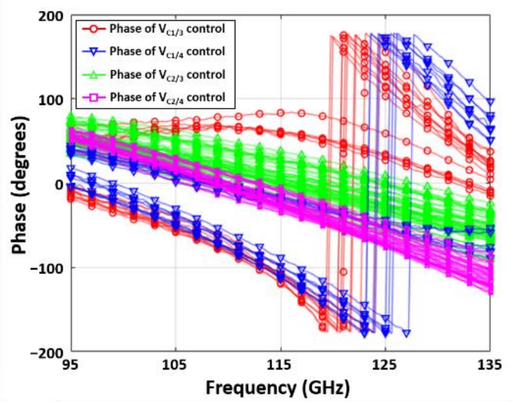
Results

● Measurement Results of Proposed Phase Shifter









Conclusion

- D-band CMOS VMPS is proposed effectively controls signal polarization in millimeter-wave imaging. The fabricated VMPS achieved a gain of -11 dB, an input P_{1dB} of 4 dBm, and consumed 22.8 mW.

Ref.	TMTT 2015	MWCL 2021	MWCL 2020	This work
Tech.	250 nm InP	55 nm BiCMOS	130 nm SiGe	65 nm CMOS
Freq. (GHz)	220–320	140–160	162–190	115–135
$\Delta\|S_{22}\|$ [a]	4 dB	3.4 dB	4.9 dB	2 dB
Gain (dB)	−13.7 ±1.9	−4.5	−6.2	−11[b]
IP_{1dB} (dBm)	−0.7	2	−13.5	7[c]
P_{dc} (mW)	21.8–42	50	9.9–15.3	36
Core Area (mm_2)	0.23	0.05	0.07	0.053

[a] Maximum Variation [b] Maximum gain [c] at 125 GHz

< Acknowledge >

- The chip fabrication and EDA tool usage were partly supported by the IC Design Education Center, Korea.