IDEC Chip Design Contest

A 389μm² 26.7nW 8-bit 100kS/s SAR ADC with Hybrid C-CI DAC

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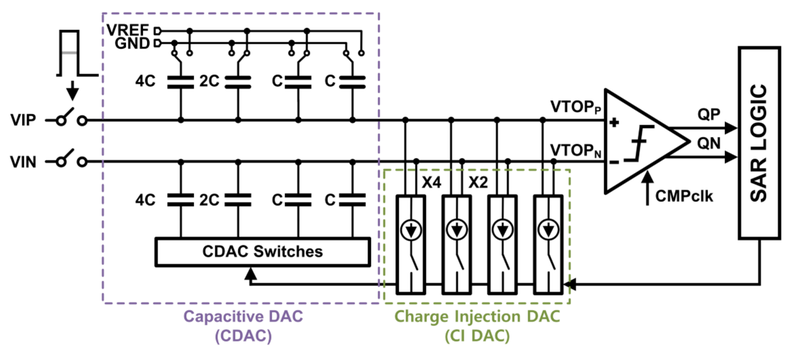
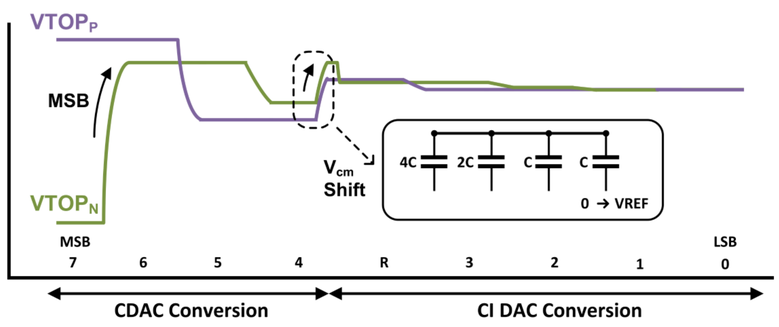
As the development of personal remote therapy systems progresses, there is increasing interest in wireless sensors for biomedical applications. Biomedical signals are characterized by small changes over a long period, and low power consumption is an important design goal for ADCs needed in implanted medical devices. This study proposes a low-power, area-efficient hybrid capacitor-charge injection DAC (C-CI DAC) SAR ADC architecture. The CI ADC, traditionally used in high-speed applications, is used at low speed and a current leakage reduction technique is introduced to reduce power consumption.

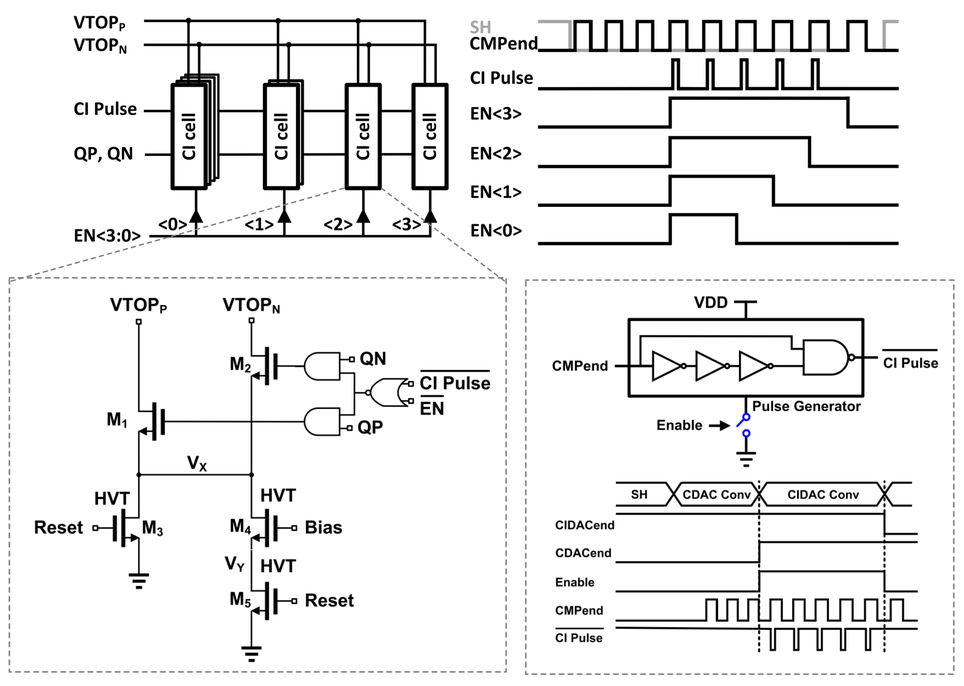
C-CI DAC-based ADC architecture





- To reduce area and power consumption:
- C-CI DAC:
  - ✓ 4bit MSB CDAC wo bridge capacitor
  - ✓ 4bit LSB CI DAC (in series)
- CDAC:
  - ✓ Converts 4 MSBs w modified monotonic switching
  - ✓ After 4 MSB conversion:
    Switches last capacitor from GND to VREF
    Ensures CI DAC operates within linear range
- CI DAC:
  - ✓ Converts lower bits
  - ✓ Redundant MSB -> mitigates gain error with CDAC
- Input switch:
  - ✓ Increased channel length reduces leakage
  - ✓ Charge-pumping lowers on-resistance

Proposed CI DAC and CI Cell



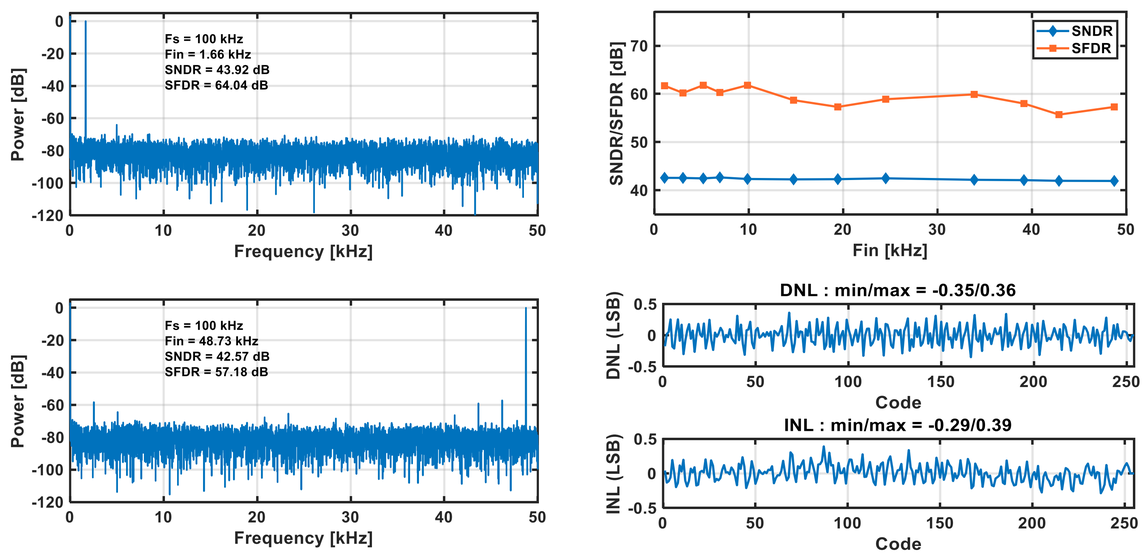
- CI DAC:
  - ✓ Consists of 8 CI cells
  - ✓ 5 conversions
- Operation:
  1) V_X and V_Y reset to 0
  2) V_Y increases until M4 turns off when a CI cell is activated
  - ✓ Injected charge determined by V_{OV} of M_4 and switches $M_{1,2}$
- Pulse Generator:
  - ✓ Requires large buffer for accuracy, causing leakage current
  - ✓ Solution: Added supply gating switch to ground connection
- Power Efficiency:
  - ✓ Conversion time: 3.65% of sampling period (50% duty cycle clock)
  - ✓ 65% power reduction in CI DAC
  - ✓ 22.77% overall ADC power reduction

Comparision Table

	This Work	ESSCIRC'23 [1]	TCAS1'18 [2]	ASSCC'17 [3]	VLSI'15 [4]
Technology [nm]	28	40	180	40	180
Architecture	C-CI	SAR+ offset-injection	SAR	SAR	Sub-ranging
Supply Voltage (V)	0.4	0.4	0.6	0.5	0.6
Sampling Rate [kS/s]	100	29	200	100	100
Resolution [bit]	8	12	10	10	8
Input Swing	±VDD	±2VDD	±VDD	NA	NA
Area [mm²]	0.000389	0.0315	0.0675	0.007	0.12
SNDR (@Nyq) [dB]	42.57	78.15	56.43	55.2	46.95
ENOB [bit]	6.78	10.56	9.08	8.87	7.5
Power [nW]	26.71	18.6	1010	69	120
FoM_W [fJ/conv-.step]	2.43	0.425	9.32	1.5	6.6

- Comparison table with ADCs for similar applications
  - ✓ Achieves 26.71nW power consumption
  - ✓ Achieves 2.43fJ/conv-step Walden FoM
  - ✓ Achieves the smallest core area of 389μm²

Measurement Results



- Left graphs
  - ✓ Shows PSD measured at 100kS/s
  - ✓ Sinusoidal input 1.66 kHz/48.73 kHz
  - ✓ Maximum SNDR: 43.92 / 42.57 dB
  - ✓ Maximum SFDR: 64.04 / 57.18 dB
- Right graphs
  - ✓ Shows SNDR and SFDR vs input frequency
  - ✓ DNL: -0.35/0.36 LSB
  - ✓ INL: 0.29/0.39 LSB

This study presents a SAR ADC with small area and low power consumption. The proposed architecture connects a CDAC and CI DAC in series and uses a minimal sampling capacitor to reduce area. By operating within the large redundancy and the linear output range of the CI cell, linearity is ensured. To reduce the power consumption of the ADC, a supply voltage on/off switch for the pulse generator and partially high threshold voltage were used. As a result, the proposed C-CI DAC SAR ADC combines the linearity and power efficiency advantages of the CDAC with the area efficiency of the CI DAC, achieving a 2.43fJ/conv-step Walden FoM and a core area of 389μm².

The chip fabrication was supported by the IC Design Education Center(IDEC), Korea.

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