

## A D-Band Frequency Doubler Based on 28-nm CMOS Technology

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Introduction

The frequency band beyond 100 GHz can be utilized for various fields such as communications, imaging, and so forth. For the implementation of high-frequency systems, a high-performance signal source is an essential component. In this work, a D-band frequency doubler is developed as a part of signal source based on 28-nm CMOS technology [1].





Fig 2. Chip photo

- Fig. 1 shows the schematic of the frequency doubler.
- A 3-stage common-source amplifier topology was adopted for the 70-GHz drive amplifier, which employs the capacitive neutralization ( $C_1-C_6$ ).
- The capacitive neutralization technique is adopted to improve high stability.
- The interstage matching networks were implementted with transformers which achieve the conjugate matching network between each stage.
- The common-source push-push structure employed for doubler.



- Fig 2. shows the chip photo of the fabricated frequency doubler.
- The size of chip is 2 1150  $\mu m^2$  including pads.
- The measurement results of frequency doubler are shown in Fig 3.
- In Fig 3. (a), peak output power is -7.5 dBm at 148 GHz with input power of 0 dBm.
- In Fig 3. (b), the saturated output power is -7.5 dBm at 148 GHz with input power of 0 dBm.
- In Fig 3. (b), peak conversion gain is 0.7 dB at 148 GHz with input power of -12 dBm.

## Conclusion

A D-band frequency doubler has been developed in this work based on 28-nm CMOS technology. It has peak output power of -7.5 dBm at 148 GHz with 0 dBm input power and saturated output power of -7.5 dBm at 148 GHz with input power of 0 dBm. The developed frequency doubler can be applied to D-band LO signal generator for wireless communication or radar system.

## Acknowledgement

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## Reference

[1] G. Lim et al., "A WR3.4 ×12 Frequency Multiplier Chain Based on InP HBT Technology," 2021 IEEE Asia-Pacific Microwave Conference (APMC), Brisbane, Australia, pp. 299-301, 2021.

