IDEC Chip Design Contest

A 240-GHz Amplifier-Frequency-Doubler Chain based on SiGe HBT Technology

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Introduction

The frequency band beyond 100 GHz can be utilized for various fields such as communication, imaging and radar systems. For the implementation of high-frequency systems, a high-performance signal source is an essential component. In this work, a 240-GHz amplifier-frequency-doubler chain is designed as a part of signal source based on IHP 130-nm SiGe HBT technology.

1. Circuit Design

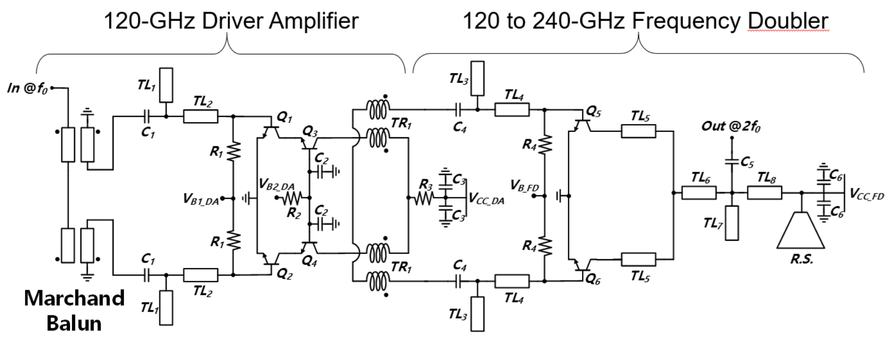

Fig. 1 Schematic of amplifier-frequency-doubler chain

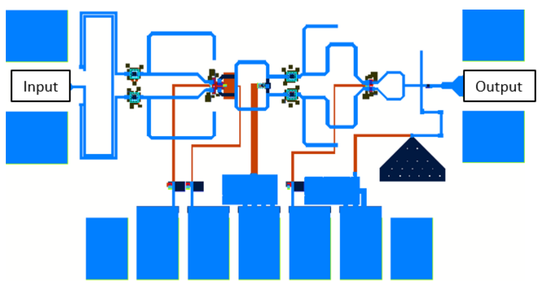

Fig. 2 Layout of amplifier-frequency-doubler chain

- Fig. 1 shows the schematic of amplifier-frequency-doubler chain (AFDC).
- Driver amplifier (DA) integrated with frequency doubler (FD) to increase the conversion gain.
- Casecode structure is adopted for DA to further increase the conversion gain.
- The common-emitter push-push structure is used for the FD which suppresses odd-harmonics and extracts 2nd harmonic signal.
- The radial stub is adopted for bypass capacitor which has high Q-factor and SRF.
- The transformer is inserted to the end of DA for inter-stage matching between the DA and the FD.
- The layout of the circuit is shown in Fig. 2.

2. Simulation Result

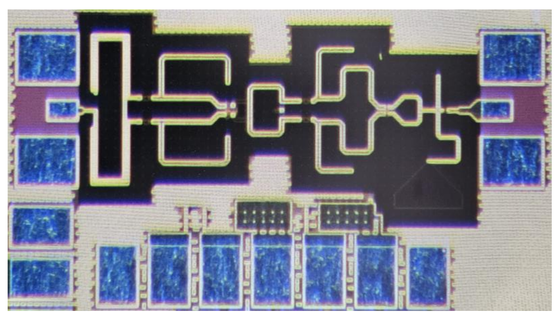

Fig. 3 Chip photo

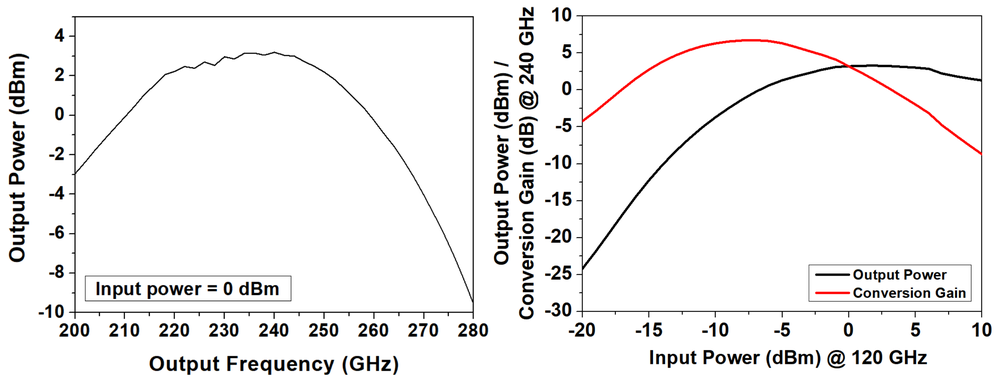

Fig. 4 Simulated result of frequency multiplier chain

- Fig.3 shows the chip photo of fabricated AFDC.
- The size of chip with DC pads is 1016 × 576 μm^2.
- The output power against output frequency is shown in Fig.4 (a), the peak output power is 3.2 dBm at 240 GHz with 0 dBm input power. The 3-dB bandwidth is 48 GHz from 210 GHz to 258 GHz.
- In Fig.4 (b), the saturated output power is 3.2 dBm at 0 dBm input power at 240 GHz. The peak conversion gain is 6.7 dB with -7 dBm input power. The fundamental frequency suppression is 20.1 dBc.
- The DC power consumption is 103.6 mW.
- The cascode stage of driver amplifier shows base-collector break down so that the measured gain shows 10 dB reduction from simulated gain.

Conclusion

In this work, 240-GHz AFDC is fabricated based on IHP 130-nm SiGe HBT technology. It has 3.2 dBm peak output power at 240 GHz with 0 dBm input power and 48 GHz 3-dB bandwidth from 210 GHz to 258 GHz. The saturated output power is 3.2 dBm at 0 dBm input power at 240 GHz. This circuit will be measured with spectrum analyzer and power meter to evaluate conversion gain and output power. The designed AFDC can be applied to wireless communication systems or radar systems.

Acknowledgement

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