IDEC Chip Design Contest

A 10T2C Capacitive SRAM-based Computing-In-Memory Macro with Array-Embedded DAC and Shift-and-Add Functions

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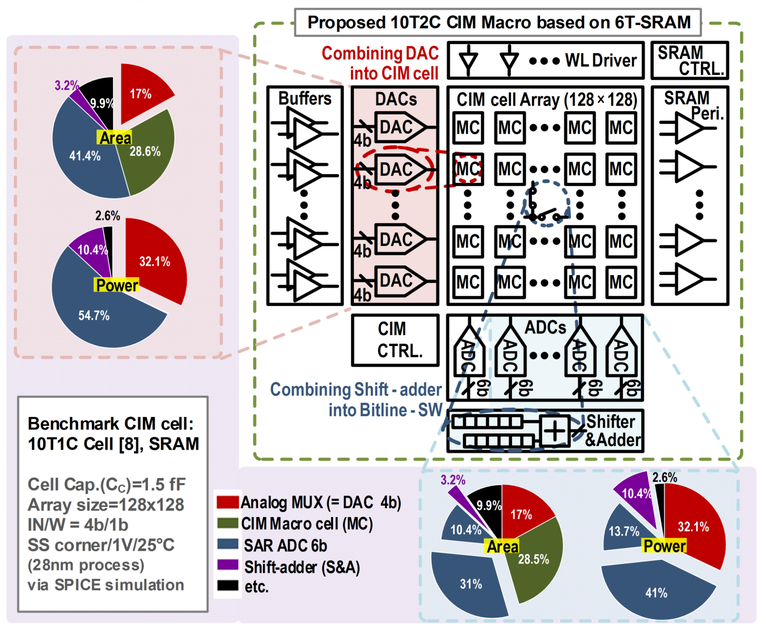
Background

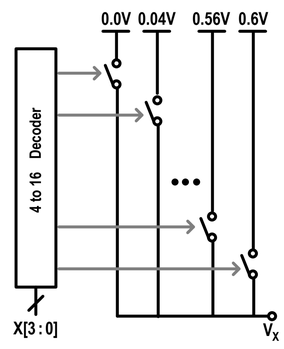
- **Large overhead of DA/AD Converter in Analog SRAM CIM**



DA/AD converter occupy 58.4% area and 86.8% power of previous 10T1C SRAM CIM array

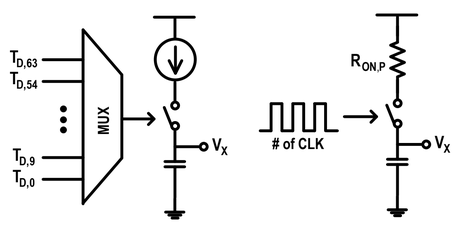
- **Previous DAC designs**

External voltage source



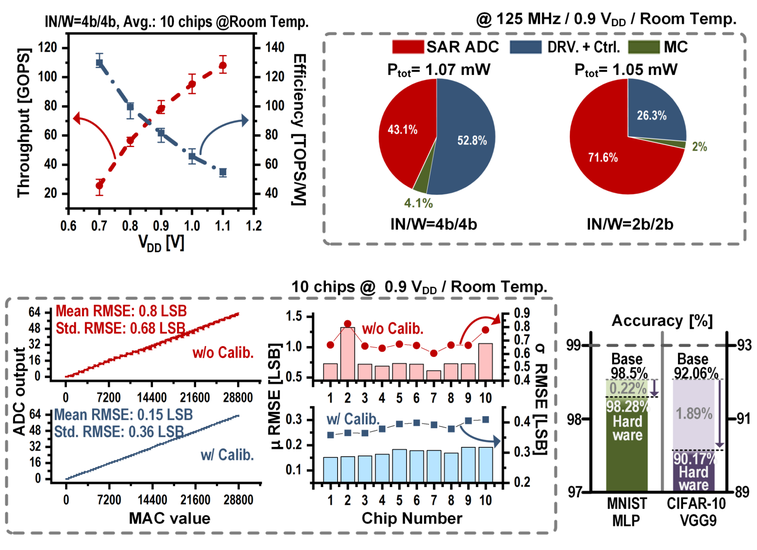
Overhead of power sources ☹

Variable pulse width



Sensitive to PVT ☹

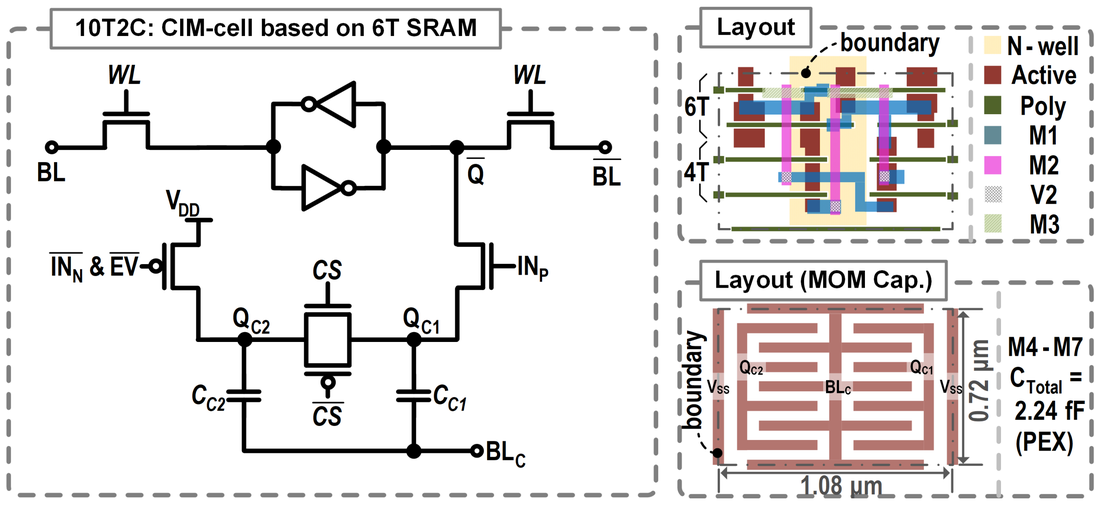
Results & Conclusion



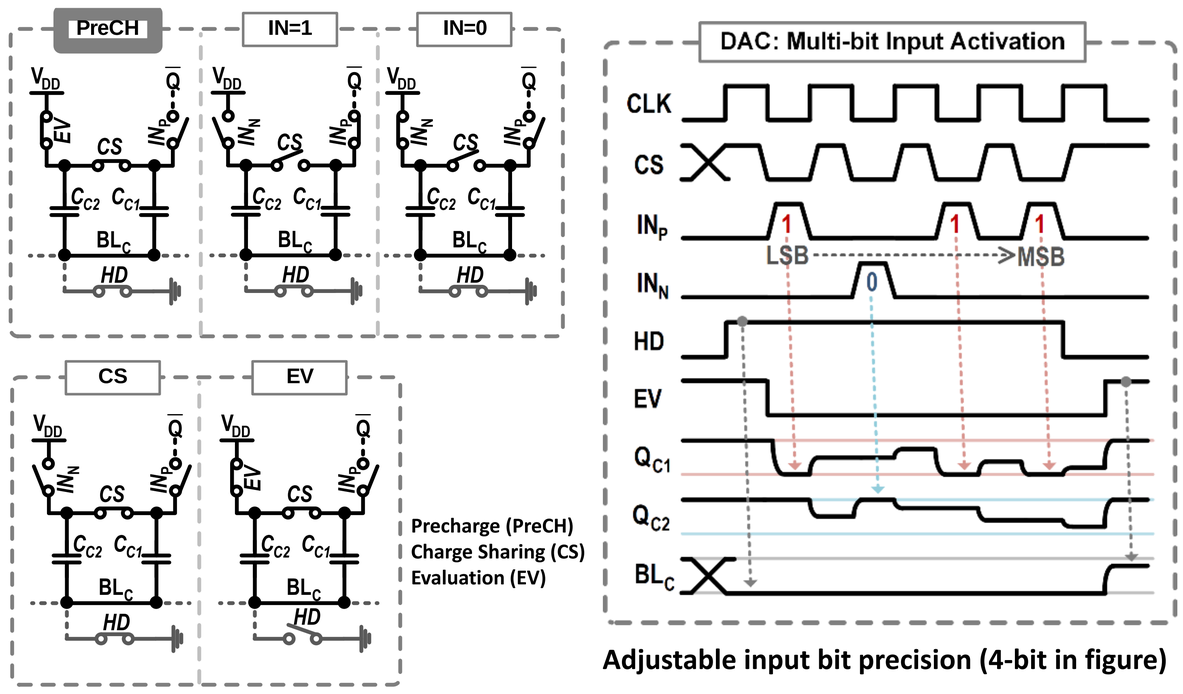
- **The proposed 10T2C CIM cell achieves increased energy efficiency and reduced area by integrating the input DAC.**
  - This approach presents an alternative to liberate from the necessity of numerous LDO regulators.
- **The embedding of the Shift-Adder in the bit-line was achieved with minor additional switches.**
  - The embedded S&A can alleviate the burden of designing ADCs with a smaller pitch and enhance energy efficiency.
- **The fabricated CIM macro achieves 130.0 TOPS/W (0.7V) and 108.1 GOPS (1.1V).**

Proposed Design

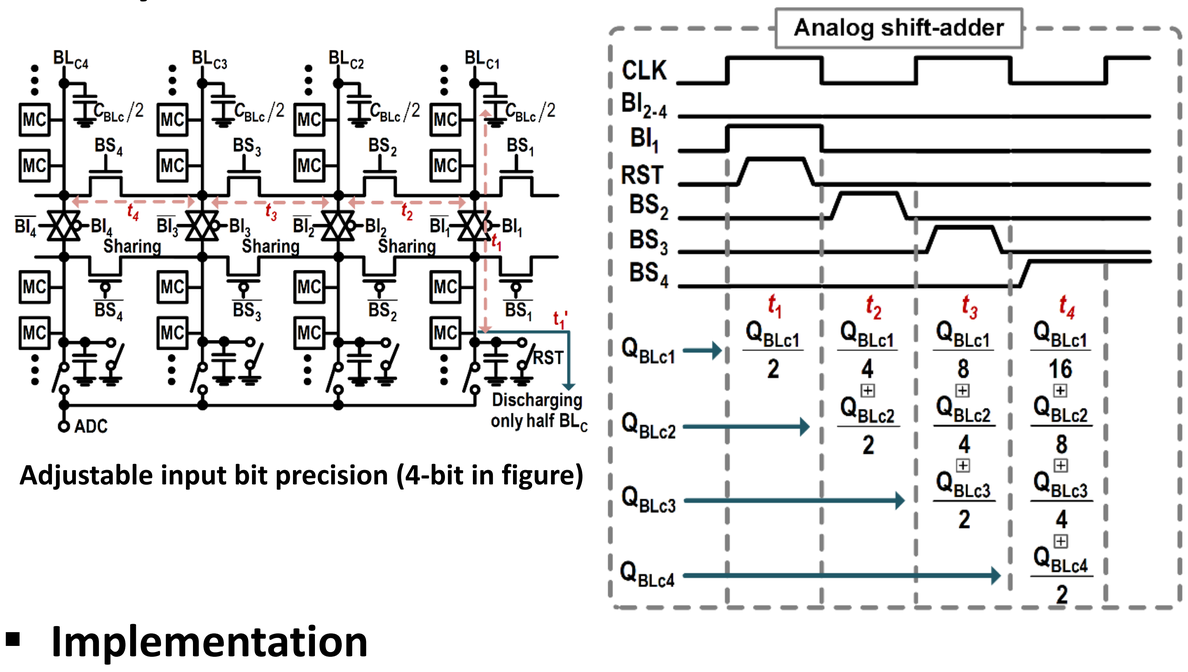
- **Proposed 10T2C SRAM cell**



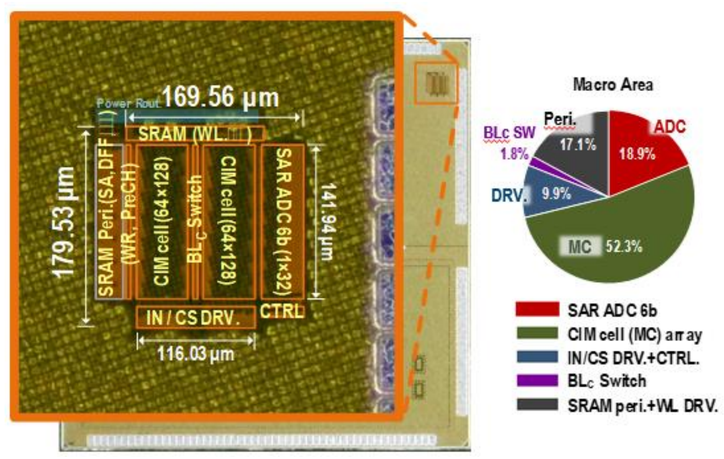
- **Array-embedded DAC function**



- **Array-embedded Shift-and-Add function**



- **Implementation**



Technology	28 nm
Macro size	128 × 128
Macro area (mm²)	0.030
Cell type	10T2C
Cell area (μm²)	0.778
Cell MoM Cap.	1.12 × 2 fF
Operation Voltage	0.7-1.1 V

This study was presented in IEEE CICC 2024.

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