IDEC Chip Design Contest

Negative Voltage Multiplier in 28 nm CMOS Process

Jae-Ho Lee, Seung-Jae Yang and Woo-Young Choi

Innovative Research Group HSCS

Introduction

- A high negative reverse bias voltage is required to operate CMOS photodetectors in the avalanche region in the 28 nm CMOS process (<-9 V).
- A negative voltage multiplier can be used to generate high negative voltage with the nominal supply voltage of MOSFET.
- This work presents an on-chip negative voltage multiplier that generates -10 V consuming 112 mW in the 28 nm CMOS process.

Negative Voltage Multiplier

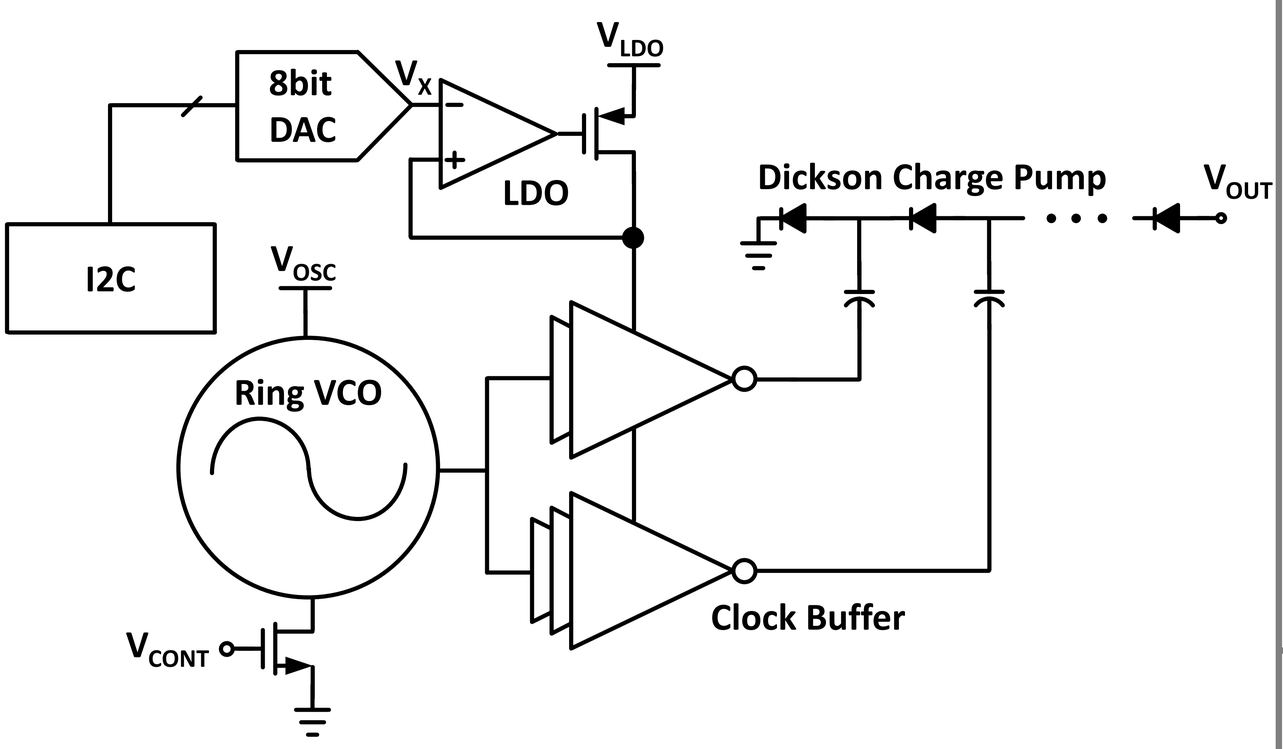

Fig. 1. Block diagram of the negative voltage multiplier

- Negative voltage multiplier includes I2C, 8-bit Digital to Analog Converter (DAC), ring Voltage Controlled Oscillator (VCO), Low Dropout Regulator (LDO), clock buffer, and Dickson Charge Pump (DCP).
- Ring VCO generates oscillating input voltage for the DCP.
- Clock buffer drives the oscillating input voltage for the DCP.
- DCP transduces the oscillating input voltage into the negative voltage.
- Cascaded DCP multiplies the generated negative voltage.

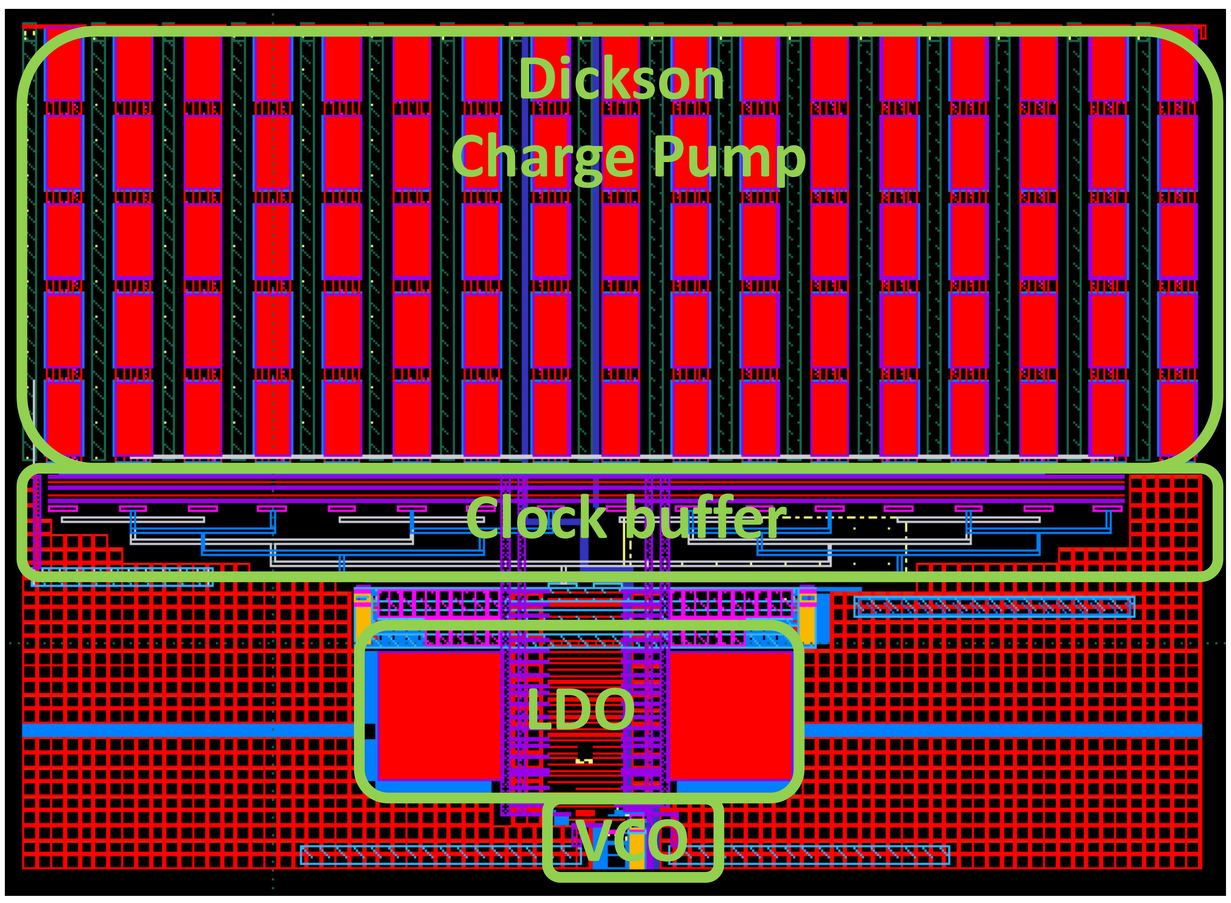

Fig. 2. Layout of the negative voltage multiplier

Chip Photograph and Measurement Setup

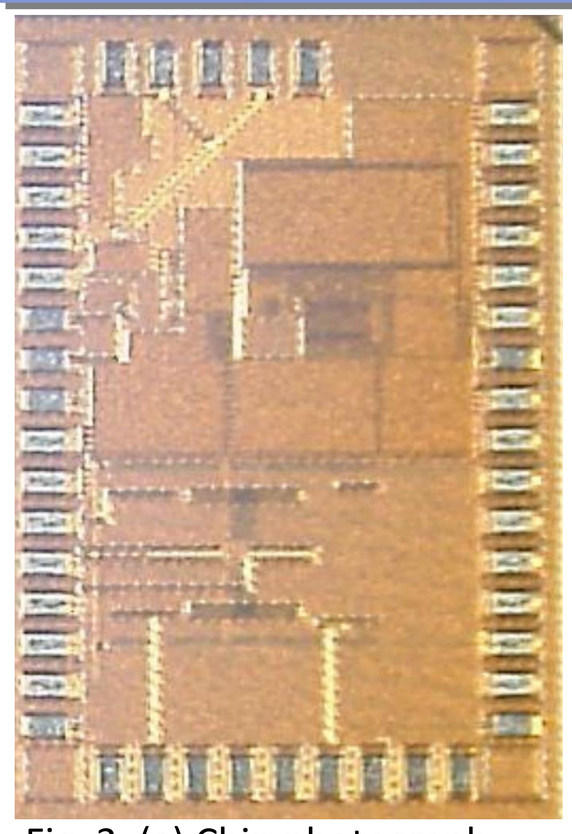

Fig. 3. (a) Chip photograph

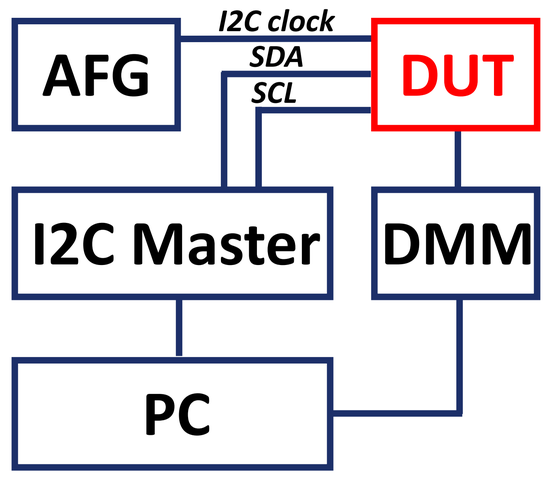

Fig. 3. (b) Measurement setup

AFG: Arbitrary Function Generator
DUT: Device Under Test
DMM: Digital Multi-Meter
I2C: Inter-Integrated Circuit
SDA: Serial Data
SCL: Serial Clock

- Fig. 3(a) shows the fabricated chip of negative voltage multiplier
- Fig. 3(b) shows the measurement setup. It consists of AFG, I2C Master, DMM, DUT, and PC.
- The DAC code sweeps automatically and the corresponding DMM results are saved accordingly.

Measurement Results

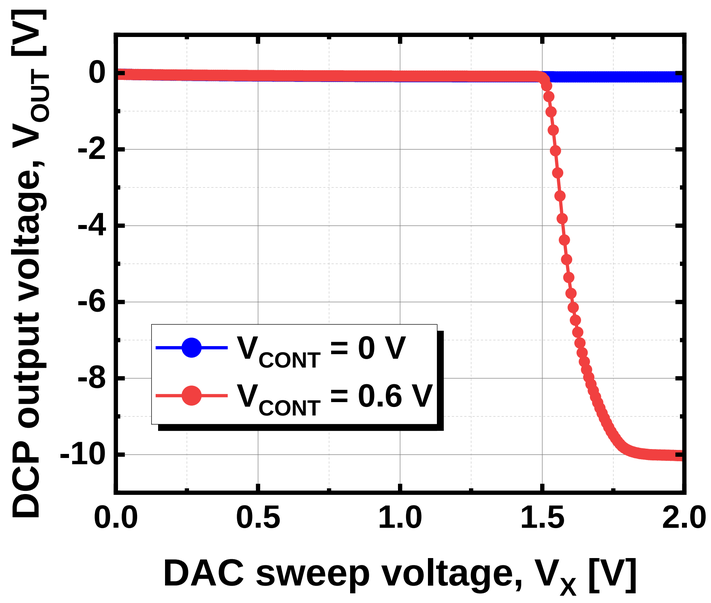

Fig. 4. Measured negative voltage multiplier output voltage as a function of the DAC sweep voltage

- - 10 V is generated with activated ring VCO.
- DAC code can be adjusted to set values in the range of 0 V to -10 V.
- It consumes 112 mW.

Conclusion

- We demonstrate on-chip negative voltage multiplier that does not exceed the nominal supply voltage of MOSFET in the 28 nm CMOS process.
- Wide range of on-chip negative voltage multiplier can be used to bias various devices such as avalanche photodetectors and single-photon avalanche diodes.

Acknowledgement

- The chip fabrication and EDA Tool were supported by IC Design Education Center(IDEC), Korea.