IDEC Chip Design Contest

High PSRR NMOS LDO Regulator With Intrinsic Gain Tracking Ripple Cancellation Technique

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INTRRODUCTION

- Several state-of-the-art techniques have been proposed to improve the PSRR performance of LDO regulators the implementation of multiple small-gain stages to increase the loop gain was utilized to enhance the PSRR performance of the LDO
- Achieving PSRR improvement becomes challenging when the feedforward gain varies with changes in VIN, output voltage (VOUT) and load current (IL). Because multi-gain stages require a large quiescent current (IQ) to maintain the high frequency of their internal non-dominant poles and feedforward technique typically requires three or more amplifiers, leading to a significant increase in IQ and design complexity.
- To overcome the drawbacks of the conventional intrinsic gain feedforward technique, the proposed LDO generates an intrinsic gain signal through MRPT configured as a source follower. furthermore, implementing the intrinsic gain tracking ripple cancellation (IGTRC) technique through MRPT and a summing amplifier (SA) effectively mitigates the DC output voltage variation of the error amplifier (VEA) caused by changes in load current (IL). This leads to a stabilized loop gain, resulting in the stabilization of the PSRR

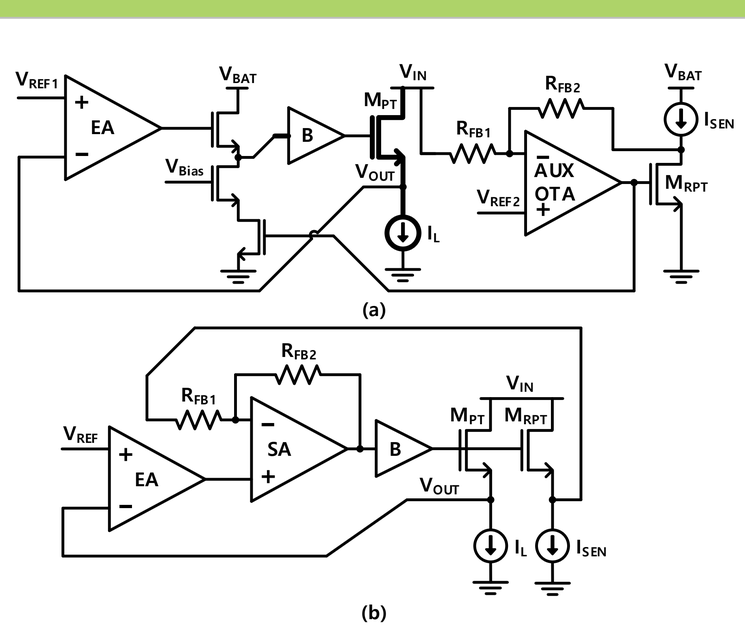

Fig. 1. Conceptial block diagram of intrinsic gain feed-forward ripple cancellation: (a) conventional LDO and (b) proposed LDO.

PROPOSED CIRCUIT DESIGN

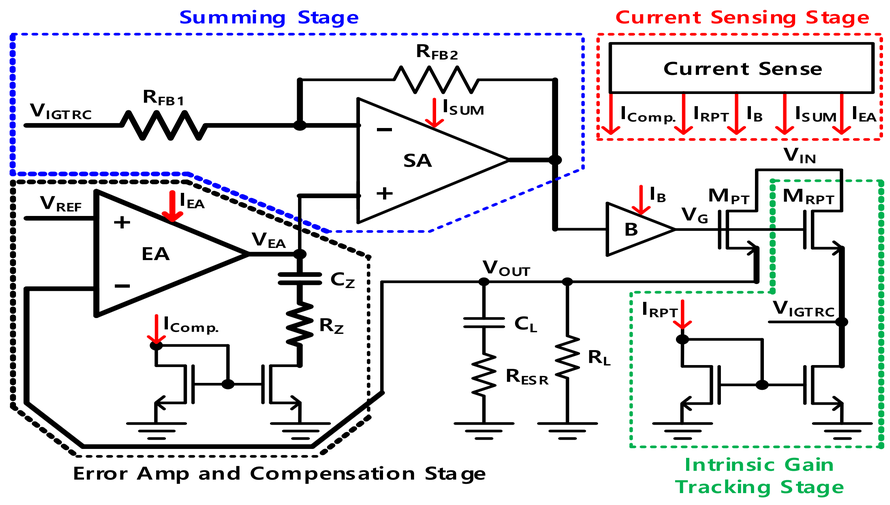

Fig. 2. Block diagram of the intrinsic gain tracking ripple cancellation technique

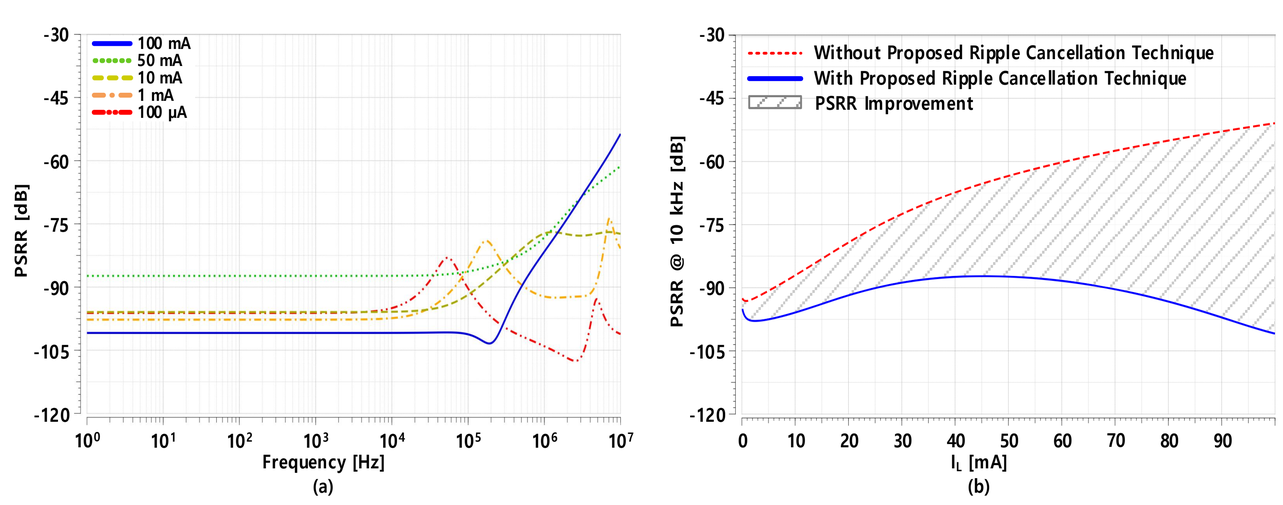

Fig. 3. PSRR post-layout simulation results of LDO for (a) proposed IGTRC, (b) improvement of PSRR with IL variation

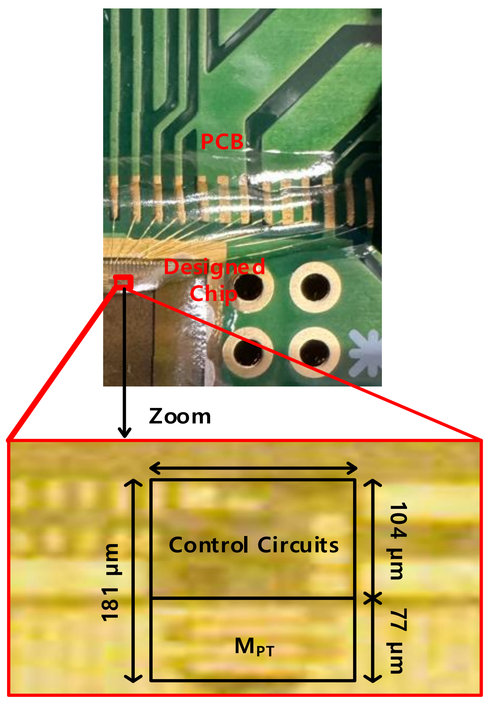

Fig. 4. Microchip photograph and test PCB.

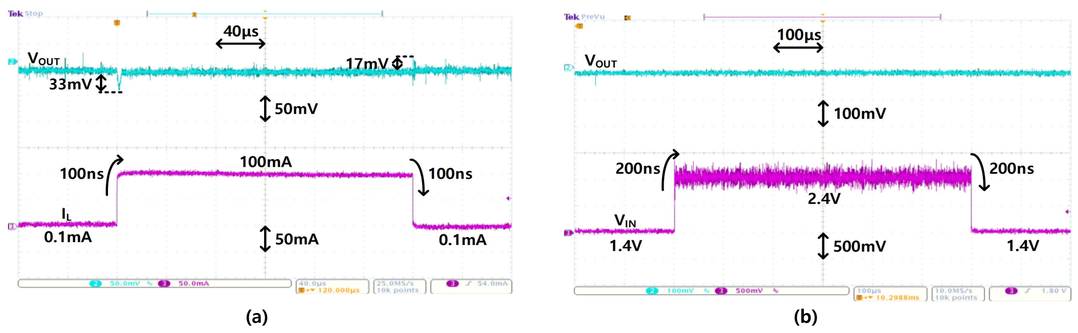

Fig. 5. Measured (a) load transient response for a IL step of 100 mA, (b) line transient response for a VIN step of 1 V (IL = 100 mA).

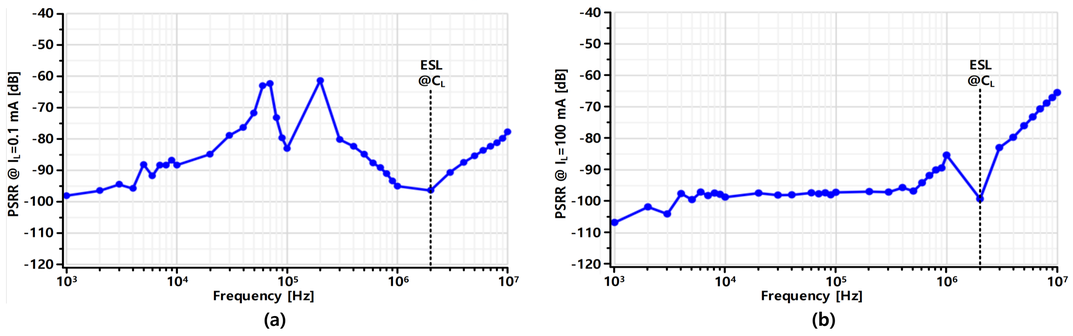

Fig. 6. Measured PSRR when (a) IL = 0.1 mA, (b) IL = 100mA

Specifications		
Technology	DB 180nm BCD	
Chip area	0.022 mm²	
VIN [V]	1.2 - 2.0	
CL [uF]	4.7	
Dropout Voltage [mV]	200	
Load Regulation [mV/mA]	0.034	
Line Regulation [mV/V]	6.83	
Overshoot Voltage[mV]	17	
Undershoot Voltage [mV]	33	
I_Q [uA]	3.7	
$PSRR@I_{Load}$:100mA	100kHz	-97dB
	1MHz	-85dB
	10MHz	-65dB
$PSRR@I_{Load}$:0.1mA	100kHz	-83dB
	1MHz	-95dB
	10MHz	-77dB

Table 1. Design result

CONCLUSION

- The proposed high PSRR LDO presents the design of the IGTRC technique. This technique uses MRPT and SA in the IGTRC loop for PSRR enhancement. The measured results verify the operation of the proposed IGTRC technique over wide ranges of IL and frequencies. As a result, the proposed LDO achieves a PSRR better than 50 dB up to 10 MHz with 3.7 µA of IQ
- The measurement results, along with the high PSRR and low IQ presented in Table I
- The chip fabrication was supported by the IC Design Education Center(IDEC), Korea.