IDEC Chip Design Contest

An 884MHz RF-DC Rectifier With −41.8dBm Input Power Sensitivity

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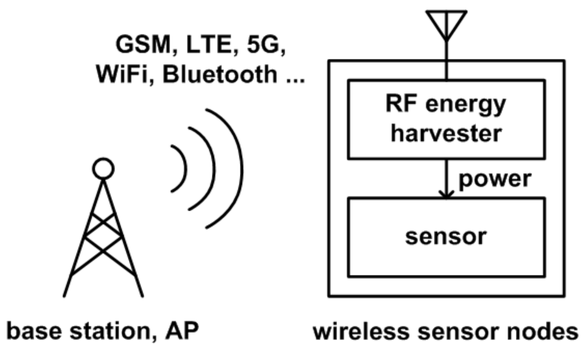
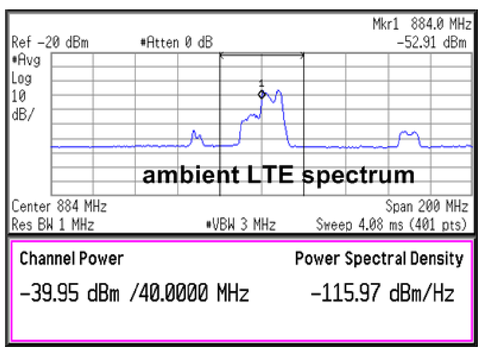
INTRODUCTION

Ambient RF Energy Harvester



Available RF Power

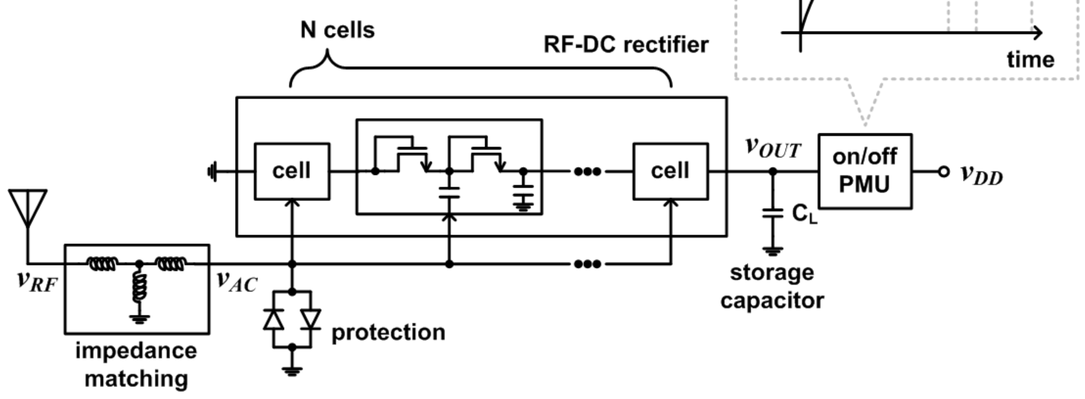


Challenge: Harvesting energy from extremely low ambient RF power

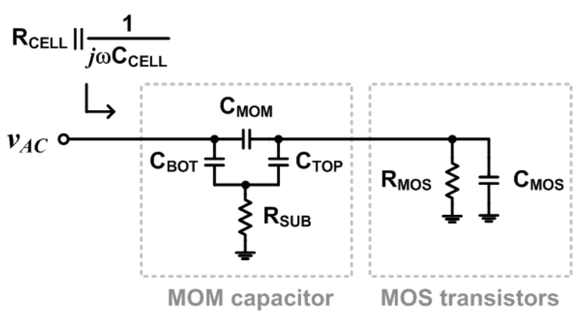
➡ Enhancing input power sensitivity of RF energy harvester

IMPLEMENTATION

Prototype RF-DC Rectifier



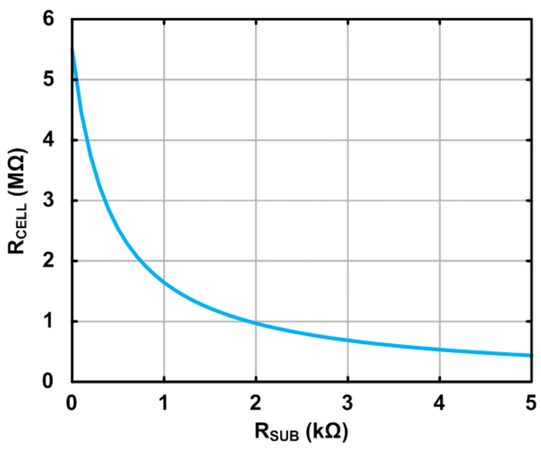
Input Impedance Model



$$R_{CELL} \approx R_{MOS} \| R_{SUB}(1+Q^2)$$

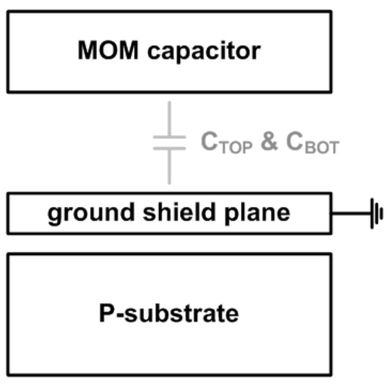
where $Q = \frac{1}{\omega(C_{TOP}+C_{BOT})R_{SUB}}$

Substrate Resistance



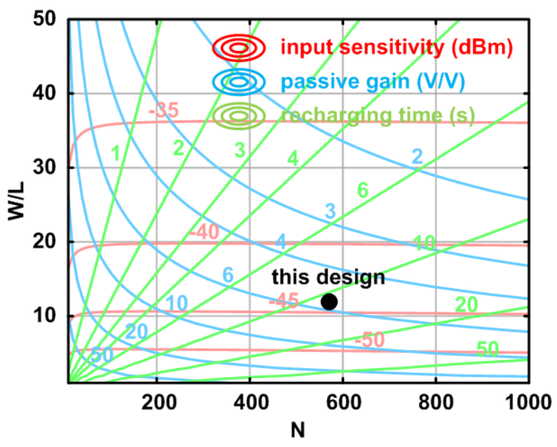
R_{CELL} increases as R_{SUB} decreases

Ground Shielded Capacitor



R_{SUB} can be decreased 84%
by using ground shield plane

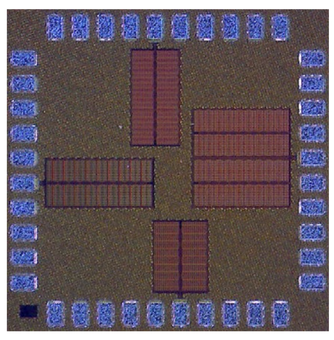
Optimization



Selected parameter: W/L=11, N=570

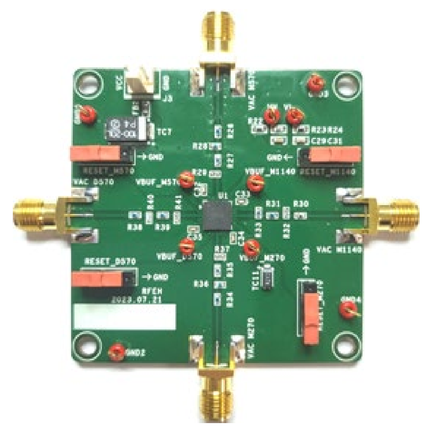
MEASUREMENT

Die Photo



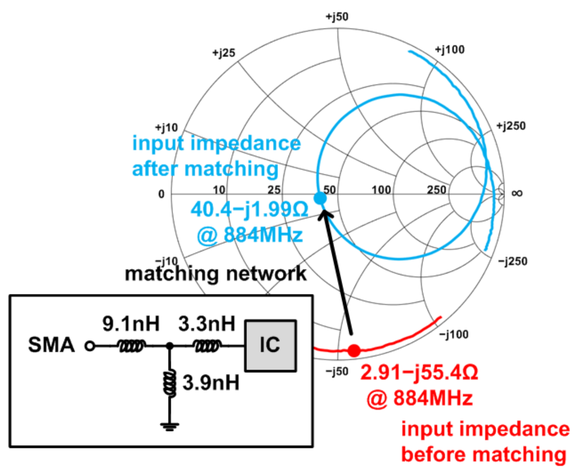
Samsung 28nm 1P11M CMOS
Active area: 217um x 379um

Test Board

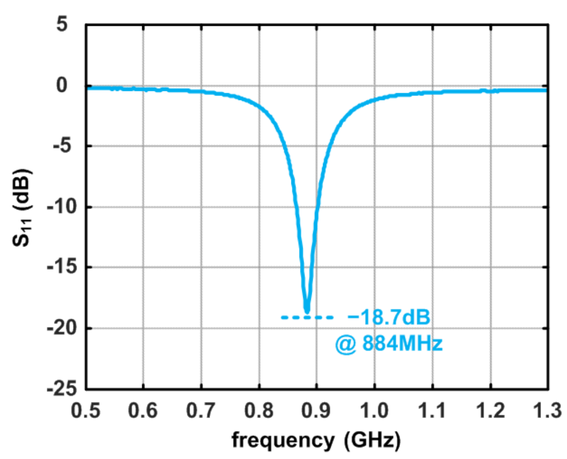


28 pin QFN 5mm x 5mm
4 layer FR4 PCB

Impedance Matching Network

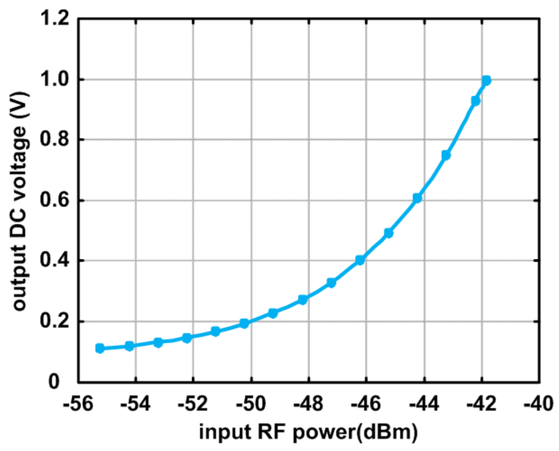


Scattering Parameter



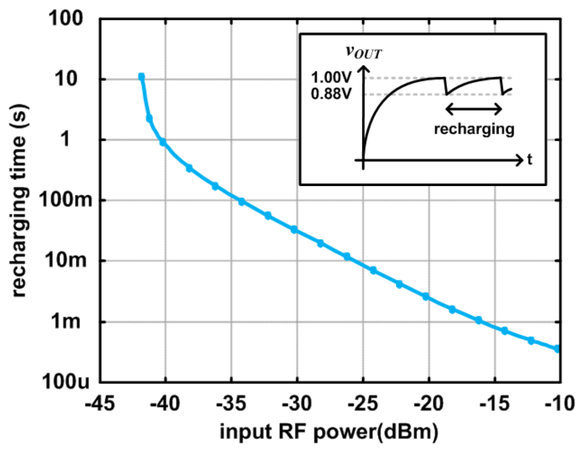
Passive amplification gain = 5.6V/V @ −40dBm −10dB bandwidth = 37.0MHz

Input Power Sensitivity



Input power sensitivity = −41.8dBm @ 1V

Recharging Time



Recharging time = 11.1s @ 1nF

CONCLUSION

Performance Summary

	JSSC 18	RFIC 12	TMTT 24	this work
CMOS technology	65nm	130nm	28nm	28nm
RF frequency	2.4GHz	0.915GHz	0.970GHz	0.884GHz
N	6	50	108	570
W/L	–	–	1/0.09	1/0.09
active die area	0.65mm^2	0.085mm^2	0.025mm^2	0.09mm^2
input sensitivity	-33dBm	-32.1dBm	-36.5dBm	-41.8dBm
output DC voltage	1V	1V	1V	1V
load resistance	∞	∞	∞	∞

Demo YouTube

with RF cable

with RF antenna

Integration of 570 rectifier cells by using ground shielded coupling capacitors

➡ Highest input power sensitivity of −41.8dBm at 884MHz

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