IDEC Chip Design Contest

A Reconfigurable 1T1C eDRAM-based Spiking Neural Network Computing-In-Memory Processor for High System-Level Efficiency

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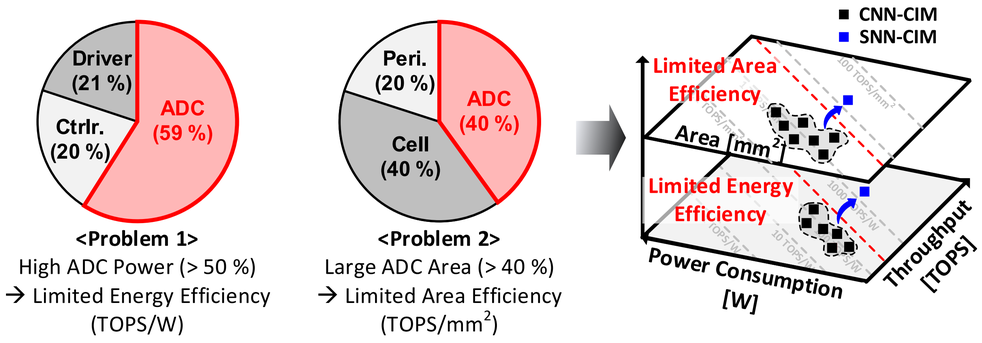
Introduction

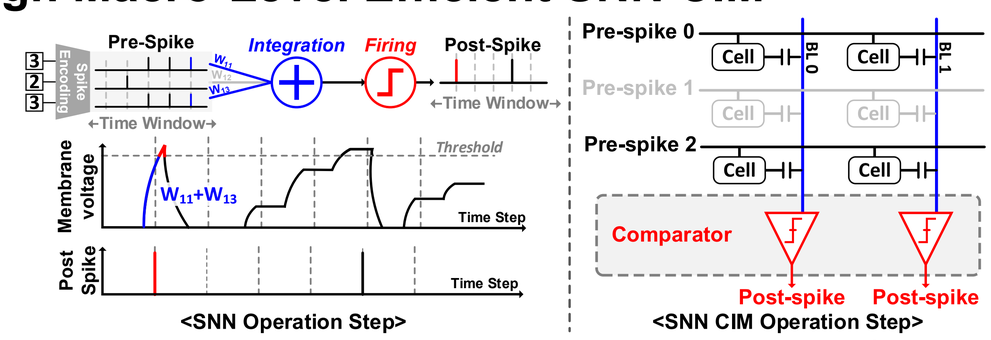
• Problems of Computing-in-Memory



<Problem 1>
High ADC Power (> 50 %)
→ Limited Energy Efficiency (TOPS/W)

<Problem 2>
Large ADC Area (> 40 %)
→ Limited Area Efficiency (TOPS/mm^2)

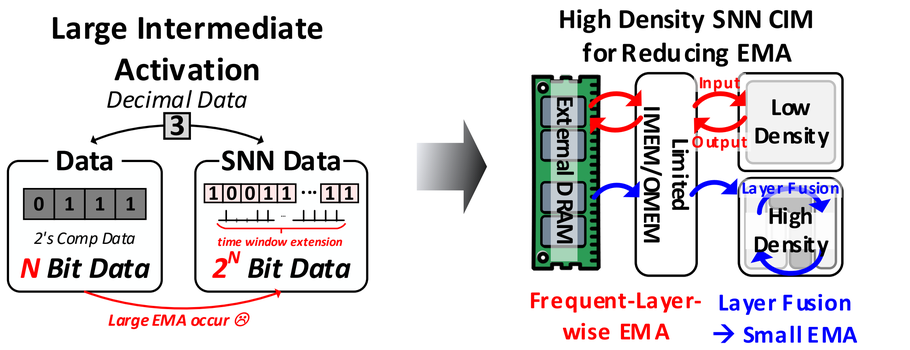
• High Macro-Level Efficient SNN CIM



<SNN Operation Step> <SNN CIM Operation Step>

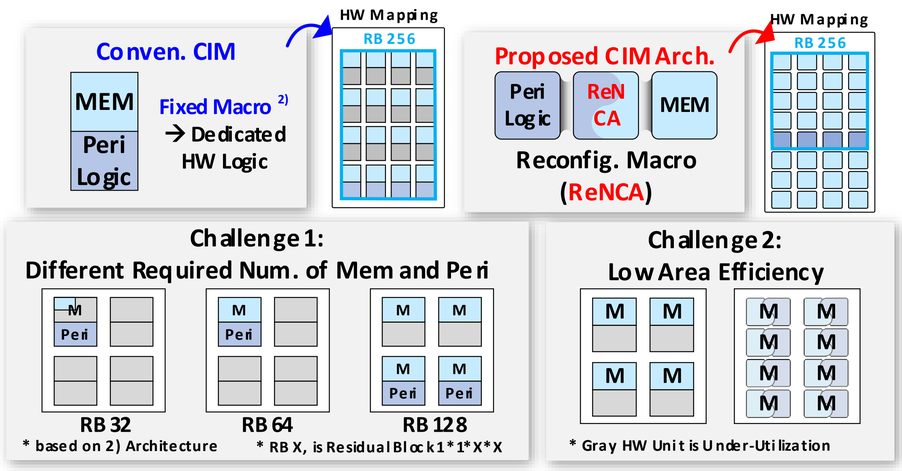
➔ ADC is not needed ➔ Power/Area Reduction ☺

• Low System-Level Efficient SNN CIM



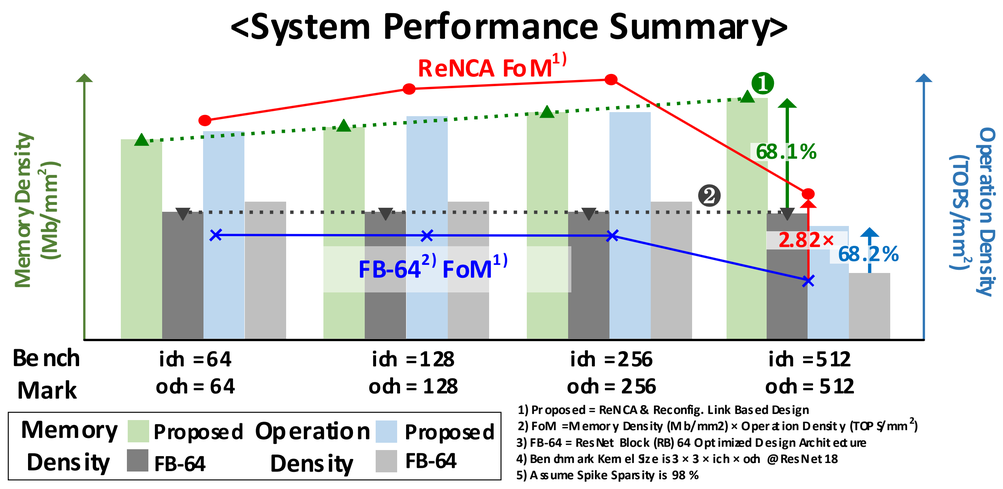
Reconfigurable Membrane Network

• Layer-wise Adaptive Accumulation Link



➔ Previous Fixed Macro Configuration
➔ HW Under-Utilization according to Various Layer Configuration
➔ Support Dynamic Accumulation & Data Path

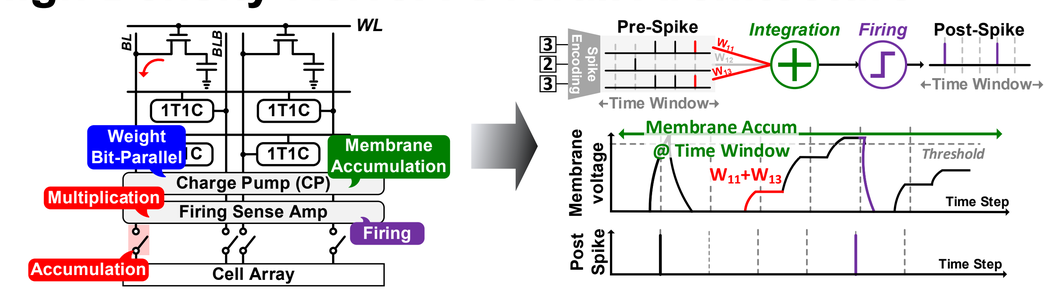
<System Performance Summary>



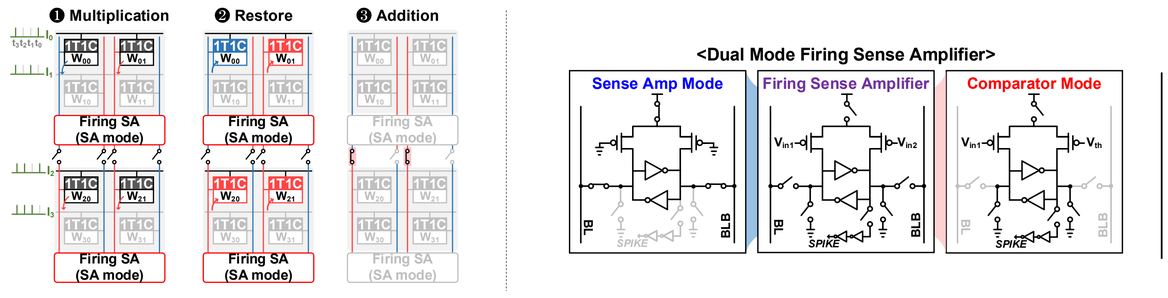
1) Proposed = ReNCA & Reconfig. Link Based Design
2) FoM =Memory Density (Mb/mm2) × Operation Density (TOPS/mm^2)
3) FB-64 = ResNet Block (RB) 64 Optimized Design Architecture
4) Benchmark Kernel Size is 3 × 3 × ich × och @ResNet18
5) Assume Spike Sparsity is 98 %

Reconfigurable Neuro-Cell Array (ReNCA)

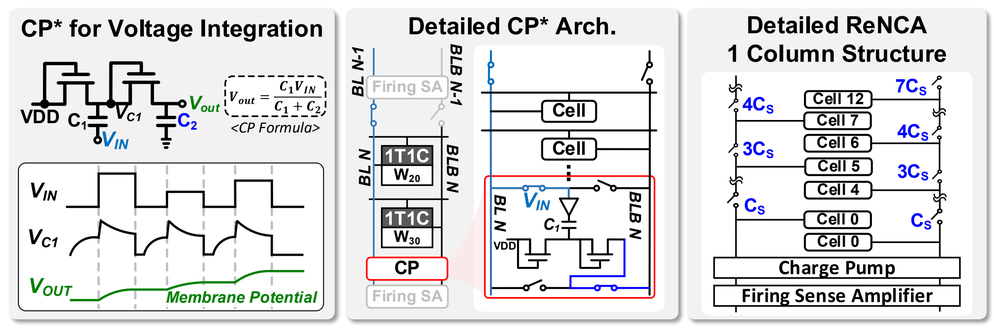
• High Density ReNCA Overall Architecture



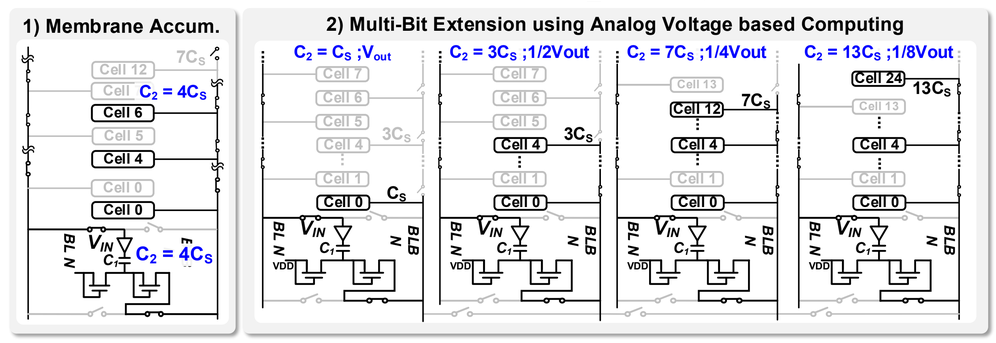
• Sense Amplifier based MAC OP. & Firing



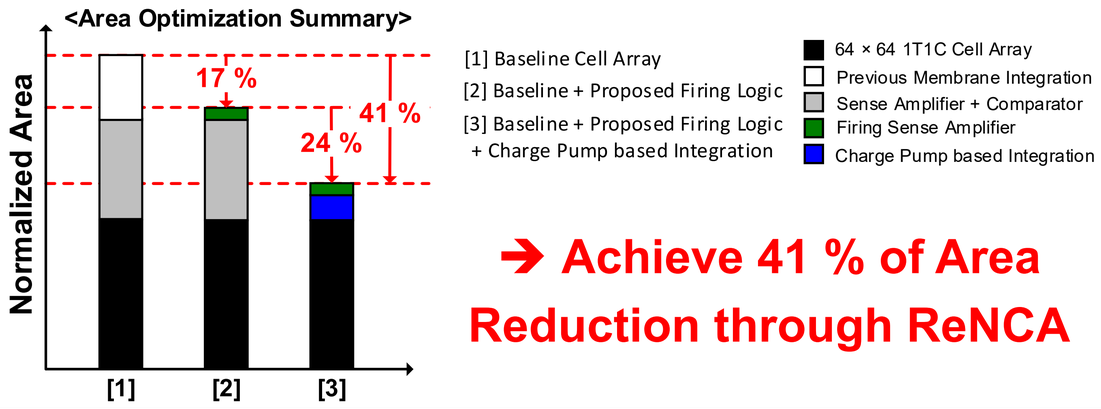
• CP* for Membrane Acc. & Multi-Bit Extension



➔ Reusing cell capacitor as CP C_2 using BL switch



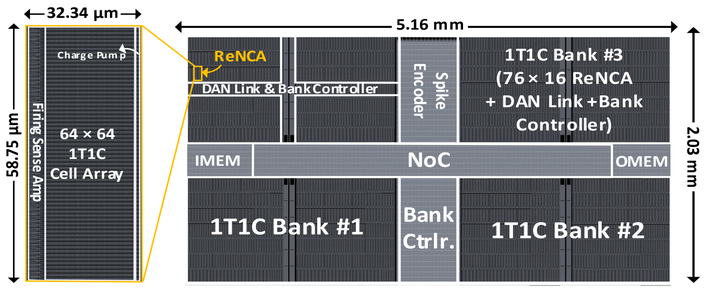
<Area Optimization Summary>



➔ **Achieve 41 % of Area Reduction through ReNCA**

Performance & Conclusion

• Chip Photograph & Performance Summary



<Performance Summary>

Technology	28 nm
Die Area	2.03 × 5.16 mm^2
Supply Voltage (V)	1.1
CIM Size (Mb)	19
Clock Frequency	250 MHz
Power (mW)	96 mW
Peak Throughput (GSOPS)	912

- 1T1C eDRAM CIM Macro for High Density
- Dynamic Adjustable Neuron Link for Reconfigurability

➔ **A 157.15 TOPS/W 1T1C eDRAM-based SNN-CIM Processor for High System-Level Efficiency**

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